
UD6810

Flash Drive Controller

Datasheet

Version 1.00

November 1, 2009

UD6810 Datasheet

Contents

1	DESCRIPTION	1
2	FEATURES	1
3	BLOCK DIAGRAM	3
4	PIN ASSIGNMENT	4
5	PIN DESCRIPTION	5
6	ELECTRICAL CHARACTERISTICS	7
6.1	ABSOLUTE MAXIMUM RATINGS	7
6.2	RECOMMENDED OPERATING CONDITIONS	7
6.3	STATIC CHARACTERISTICS	7
6.4	AC CHARACTERISTICS	7
7	TYPICAL APPLICATION	10
8	MECHANICAL DIMENSIONS	11
8.1	LQFP 48-PIN UD6810 PACKAGE OUTLINE DIMENSION	11
8.2	TQFP 48-PIN UD6810 PACKAGE OUTLINE DIMENSION	12

UD6810 Datasheet

1 Description

UD6810 is an advanced Hi-speed USB flash drive controller intended for supporting flash memory device. It provides enhanced read/write and power performance. With flexible firmware code design technology, UD6810 can support comprehensive Flash technologies, including Single-Level Cell (SLC), Multi-Level Cell (MLC), Three-Level Cell (TLC), AG-AND, AND, and Nor Flash memory. It allows the manufacturer to improve device performance and maximize flexibility in flash decision.

The on-the-fly ECC engine is capable of correcting up to 48 bits errors per 1024 bytes. For data security, UD6810 are designed with Data-Safe technology to prevent data corruption even if it is powered off or unplugged during data transfer, UD6810 is the most power efficient solution for manufacture.

UD6810 is a highly integrated single chip for USB2.0 flash drive controller, it integrates USB2.0 Transceiver Macro cell Interface (UTMI), the Serial Interface Engine (SIE), one cycle compatible micro-controller and voltage regulators. The highly integration reduces overall cost by minimizing component amount. UD6810 is Employed leading 0.18um CMOS technology.

UD6810 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, UD6810 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, Drive partitions, password check for security Drive, are available as part of our mass production software package.

UD6810 are available in 48-pin LQFP/TQFP package. The 48-pin UD6810 supports up to 8 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

■ USB Interface

High-speed USB 2.0 interface; backward compatible with USB 1.1
Integrated USB 2.0 Transceiver Macro cell Interface (UTMI) and Serial Interface Engine (SIE)

■ Flash Interface

NAND flash: x8,

SLC, MLC, TLC

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All kinds of flash CMOS technology: 2xnm, 3xnm, 4xnm, 5xnm, 7xnm, 9xnm etc.

AG-AND flash

AND flash

NOR flash

■ Flexible Firmware Update

Flexible firmware code design to support various new flash memories

■ On-the-fly 48 bit/1024 byte, ECC built-in Hardware enhances reliability

■ Micro-controller with enhanced feature

One clock per instruction cycle

Embedded RAM and ROM

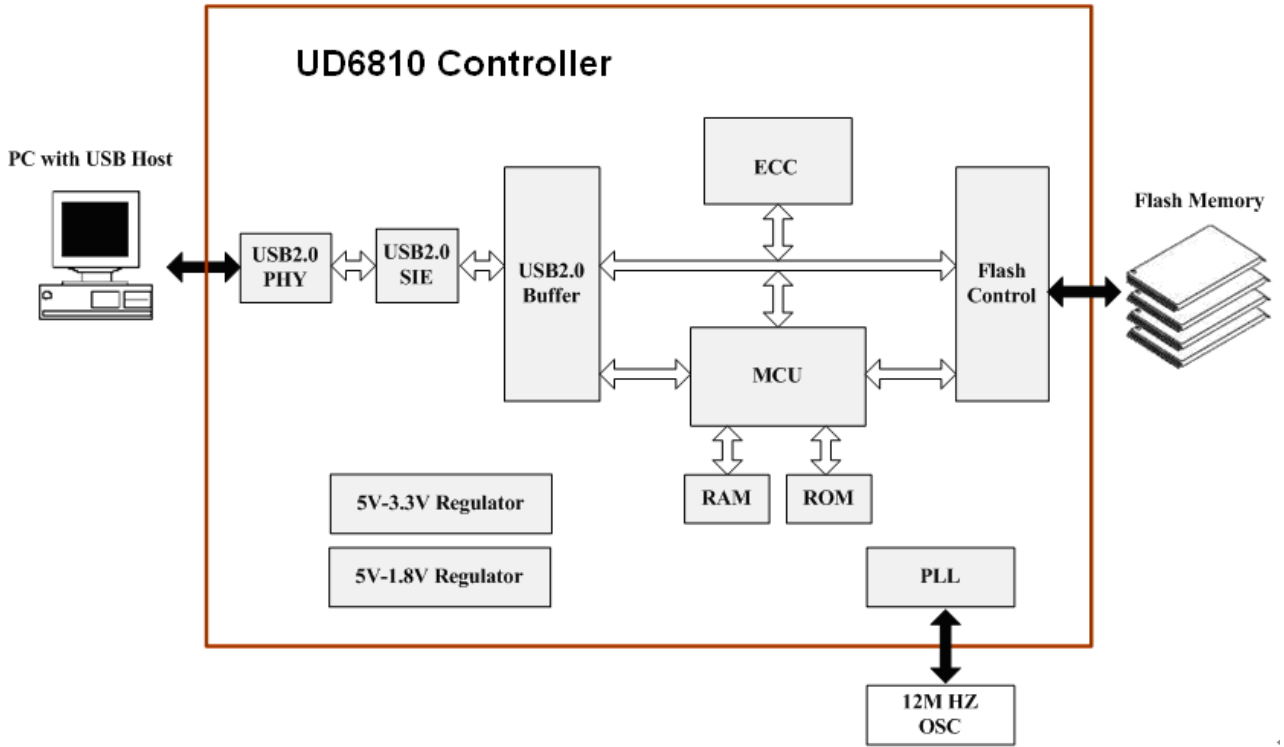
■ Data-Safe Protection Technology

Prevent data corruption even if it is powered off or unplugged during data transfer.

UD6810 Datasheet

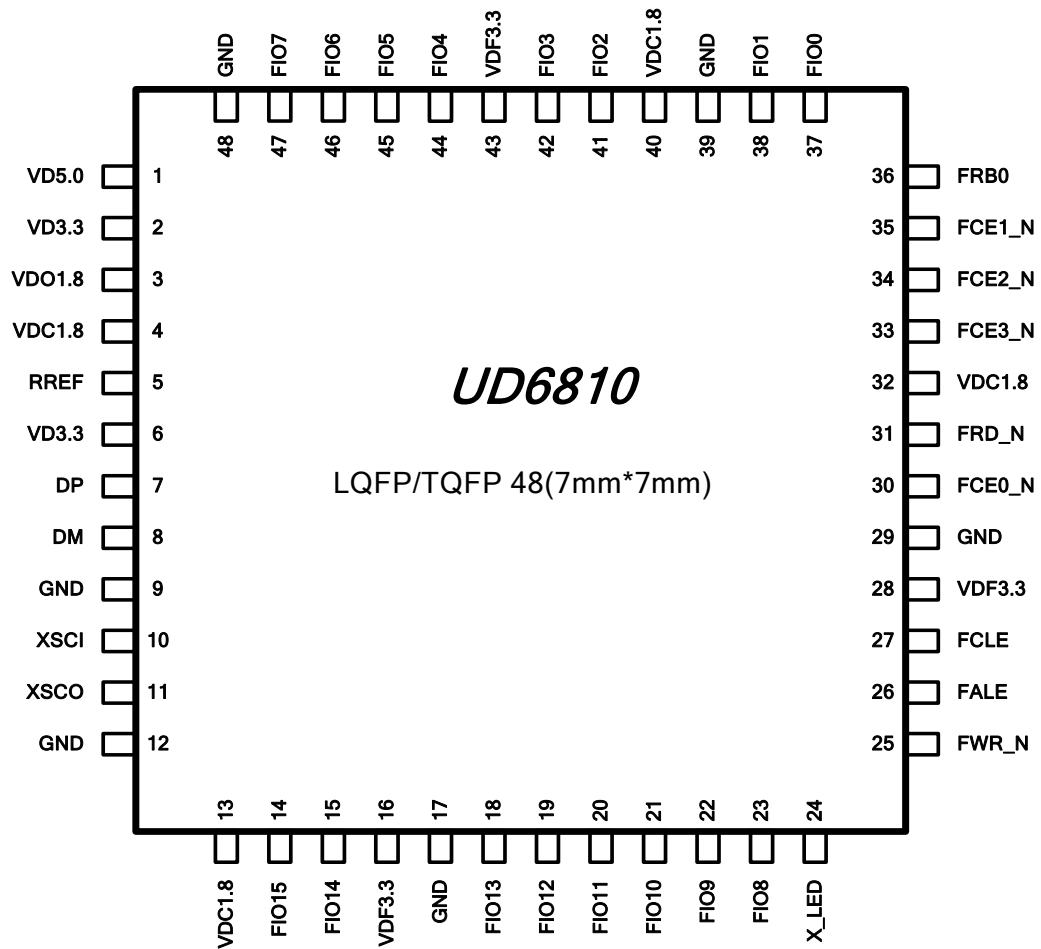
- **High data transfer rate with Multi-Plane and Interleave technology**
- **Design For Secondary Development**
 - Support composite device
 - Support HID device and Mass Storage Device with one device address
 - Support predefined and user defined private command for HID and Mass Storage Device
- **Independent HID device support**
 - HID device for USB-Key Application
 - HID device for low speed USB adapter (e.g. USB to RS232 and others)
- **Integrated 5v to 3.3v & 5v to 1.8v voltage regulator**
- **LED indicator shown three different access status: Busy, Waiting, and Off**
- **Drive partitions and password check for security drive**
- **PC boot up as USB Zip Drive or USB Hard Drive**
- **Auto run function**
- **Customized VID/PID and serial number**
- **USB suspend and resume**
- **Low power dissipation**
- **0.18um CMOS technology, 1.8 Volt low power core operation**
- **7 mm x7mm 48-pin LQFP/TQFP**
- **Supports up to 8 Flash Chips**
- **Windows, Mac and Linux kernel 2.4 above compatible**

3 Block Diagram



4 Pin Assignment

LQFP/TQFP48 (Top Side)



5 Pin Description

Brief UD6810 pin functions are shown in the following tables.

- I** : Input signal
- O** : Output signal
- I/O** : Bi-direction signal
- PWR** : Power signal
- GND** : Ground signal

UD6810 LQFP/TQFP 48 Pin Description

LQFP 48 Pin NO.	Pin Name	Type	Description
1	VD5.0	I	Regulator 5.5V Power Input
2	VD3.3	PWR	Regulator 3.3V Out
3	VDO1.8	PWR	Regulator 1.8V Out
4	VDC1.8	PWR	1.8V core logic power supply
5	RREF	I	Connect External Resister for current reference
6	VD3.3	PWR	Regulator 3.3V Out
7	DP	I/O	USB Data D+
8	DM	I/O	USB Data D-
9	GND	GND	Ground
10	XSCI	I	Crystal Input (12 MHz)
11	XSCO	O	Crystal Output
12	GND	GND	Ground
13	VDC1.8	PWR	1.8V core logic power supply
14	FIO15	I/O	Flash Data Bus - bit 15
15	FIO14	I/O	Flash Data Bus - bit 14
16	VDF3.3	PWR	3.3V flash I/O pad power supply
17	GND	GND	Ground
18	FIO13	I/O	Flash Data Bus - bit 13
19	FIO12	I/O	Flash Data Bus - bit 12
20	FIO11	I/O	Flash Data Bus - bit 11
21	FIO10	I/O	Flash Data Bus - bit 10
22	FIO9	I/O	Flash Data Bus - bit 9
23	FIO8	I/O	Flash Data Bus - bit 8
24	X_LED	I/O	LED indicator
25	FWR_N	O	Flash Write Enable (active low)
26	FALE	O	Flash Address Latch Enable
27	FCLE	O	Flash Command Latch Enable
28	VDF3.3	PWR	3.3V flash I/O pad power supply

UD6810 Datasheet

29	GND	GND	Ground
30	FCE0_N	O	Flash Chip Enable 0 (active low)
31	FRD_N	O	Flash Read Enable (active low)
32	VDC1.8	PWR	1.8V core logic power supply
33	FCE3_N	O	Flash Chip Enable 3 (active low)
34	FCE2_N	O	Flash Chip Enable 2 (active low)
35	FCE1_N	O	Flash Chip Enable 1 (active low)
36	FRB0	I	Flash Ready Busy
37	FIO0	I/O	Flash Data Bus - bit 0
38	FIO1	I/O	Flash Data Bus - bit 1
39	GND	GND	Ground
40	VDC1.8	PWR	1.8V core logic power supply
41	FIO2	I/O	Flash Data Bus - bit 2
42	FIO3	I/O	Flash Data Bus - bit 3
43	VDF3.3	PWR	3.3V flash I/O pad power supply
44	FIO4	I/O	Flash Data Bus - bit 4
45	FIO5	I/O	Flash Data Bus - bit 5
46	FIO6	I/O	Flash Data Bus - bit 6
47	FIO7	I/O	Flash Data Bus - bit 7
48	GND	GND	Ground

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions	min	max	unit
VCCA	analog supply voltage		-0.5	5.5	v
VCCD	digital supply voltage		-0.5	4.5	v
VI	input voltage		-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A			v
			DP, DM and GND pins	-4000	
			other pins	-2000	+2000
Tstg	storage temperature		-40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VCCA	analog supply voltage		3.0	3.3	3.6	V
VCCD	digital supply voltage		3.0	3.3	3.6	V
VI	input voltage		0	-	VCCD	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	°C

6.3 Static characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = 40 to 85 °C;

symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode	-	500		uA

6.4 AC characteristics

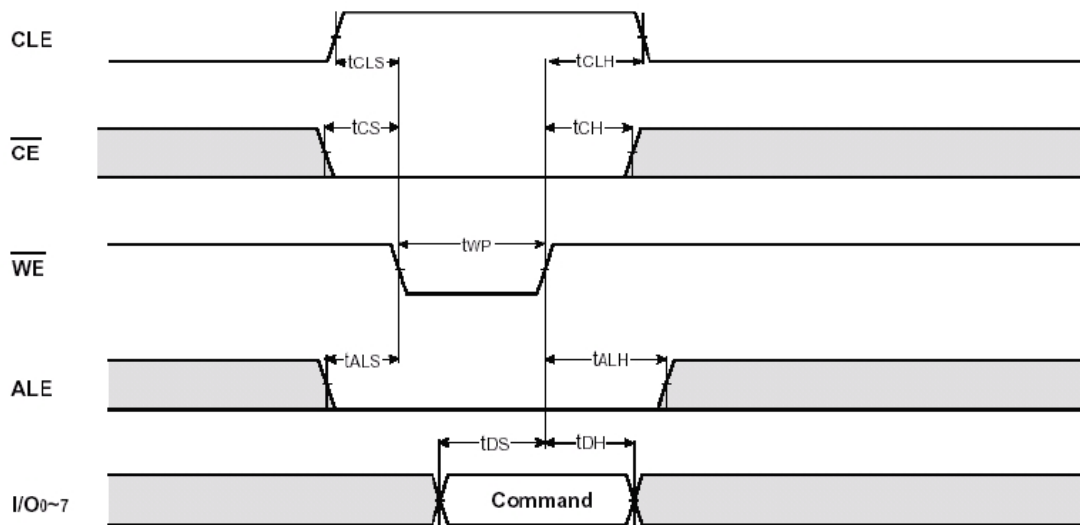
NAND Flash Memory Interface Timing

symbol	Parameter	Min	Max	Unit
t _{CLS}	CLE Set-up Time	16	-	ns
t _{CLH}	CLE Hold Time	33	-	ns
t _{CS}	CE Set-up Time	33	-	ns
t _{CH}	CE Hold Time	16	-	ns
t _{wp}	WE Pulse Width	16	-	ns
t _{ALS}	ALE Set-up Time	16	-	ns

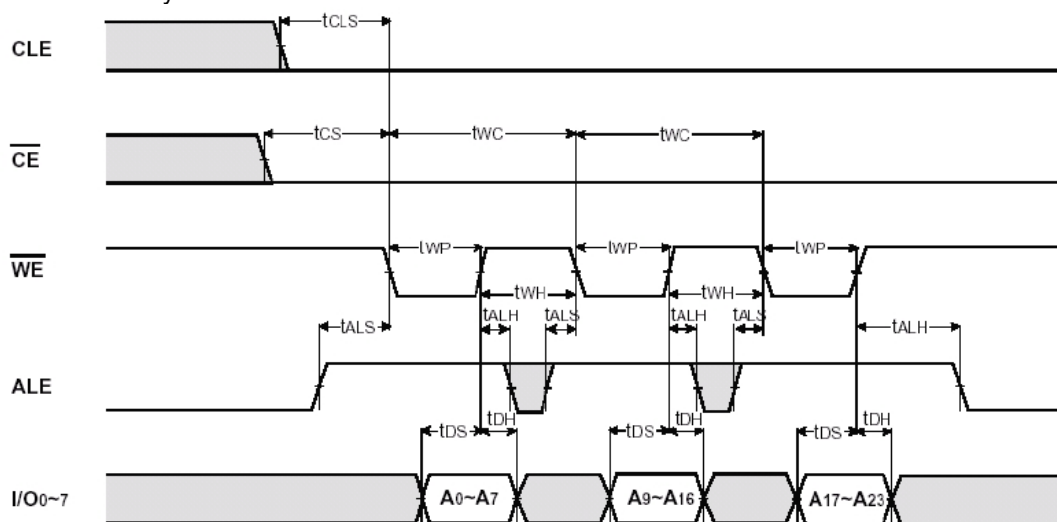
UD6810 Datasheet

t_{ALH}	ALE Hold Time	33	-	ns
t_{DS}	Data Set-up Time	15	-	ns
t_{DH}	Data Hold Time	8	-	ns
t_{WC}	Write Cycle Time	25	-	ns
t_{WH}	WE High Hold Time	8	-	ns
t_{RC}	Read Cycle Time	25	-	ns
t_{RP}	/RE Pulse Width	16	-	ns
t_{REH}	/RE High Hold Time	8	-	ns
t_{RR}	Read to /RE low	66	-	ns

Command latch cycle

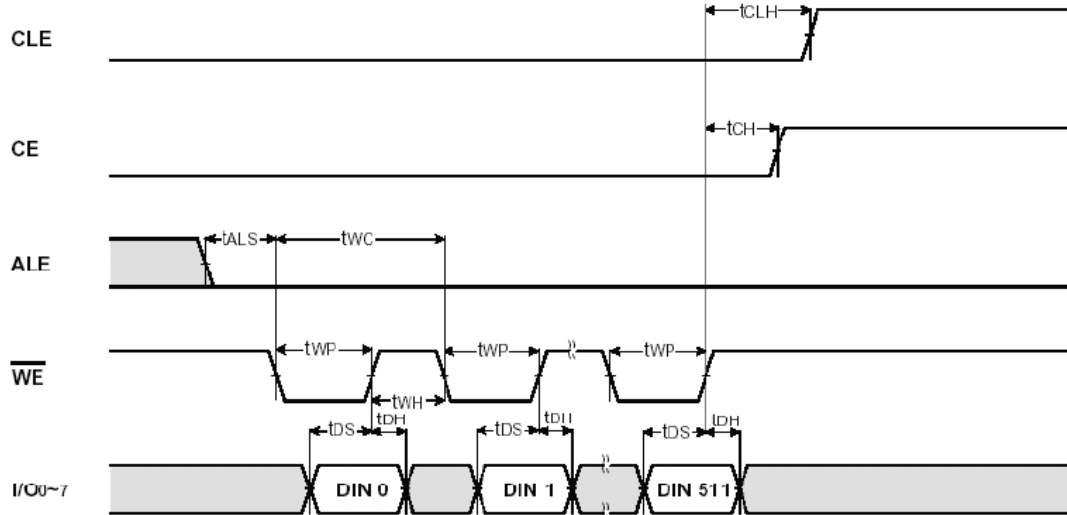


Address latch cycle

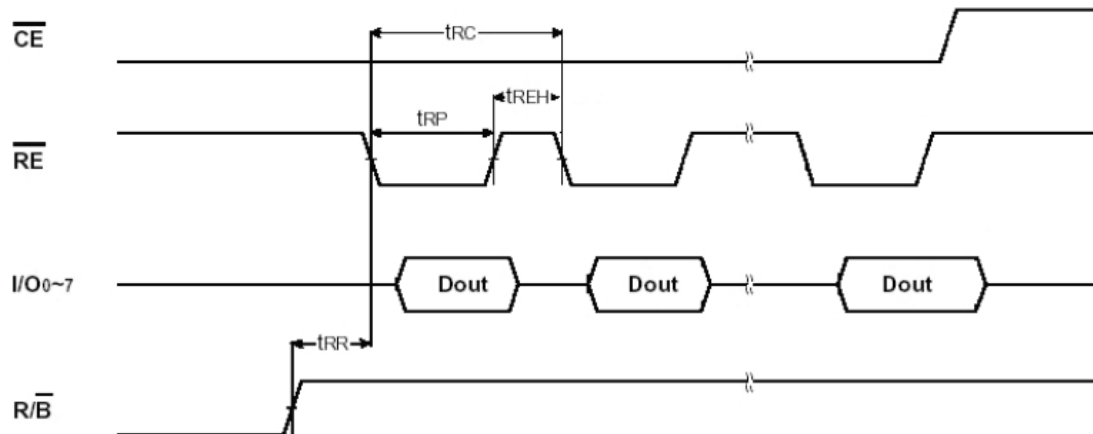


UD6810 Datasheet

Input Data latch cycle

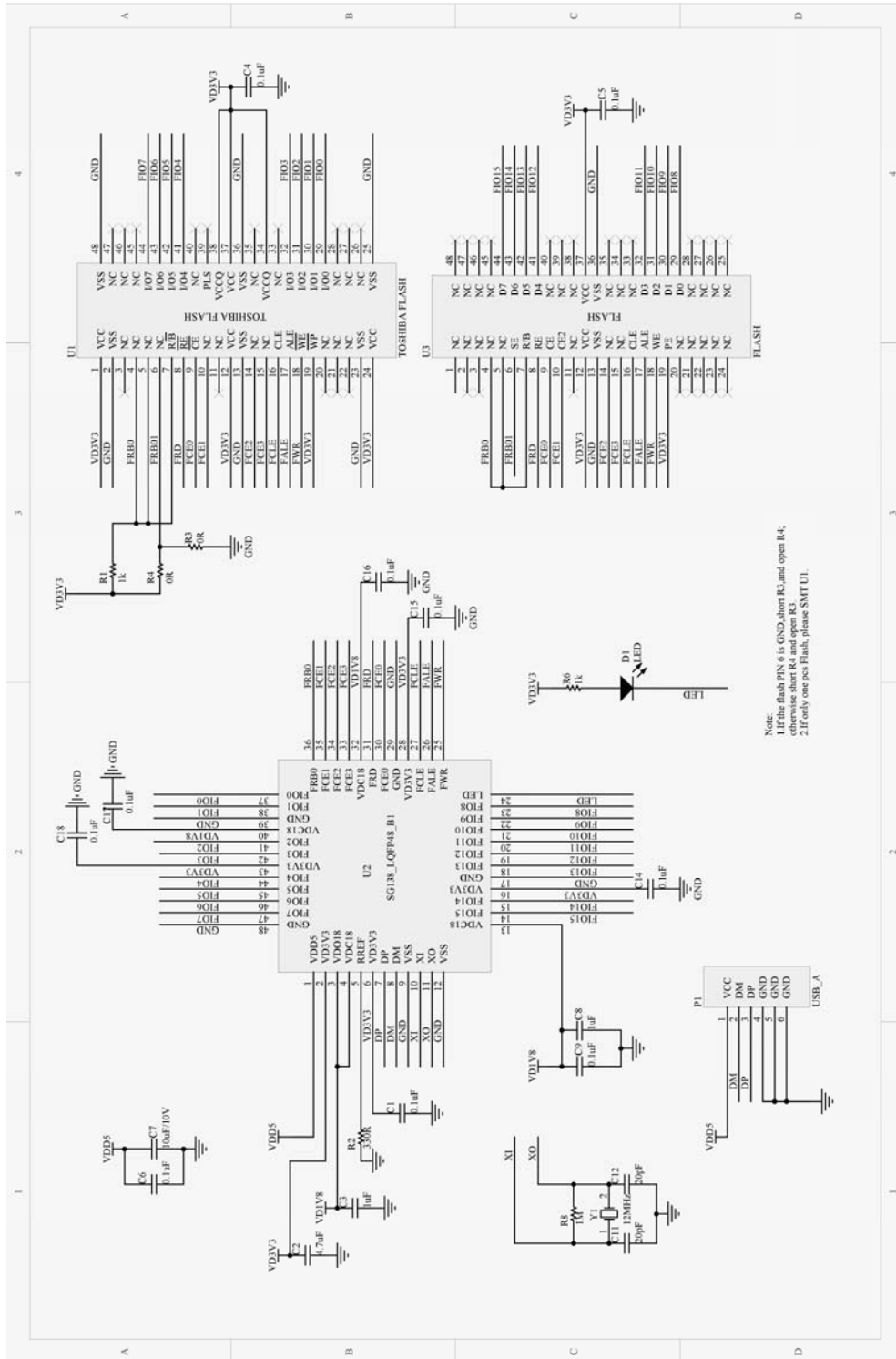


Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



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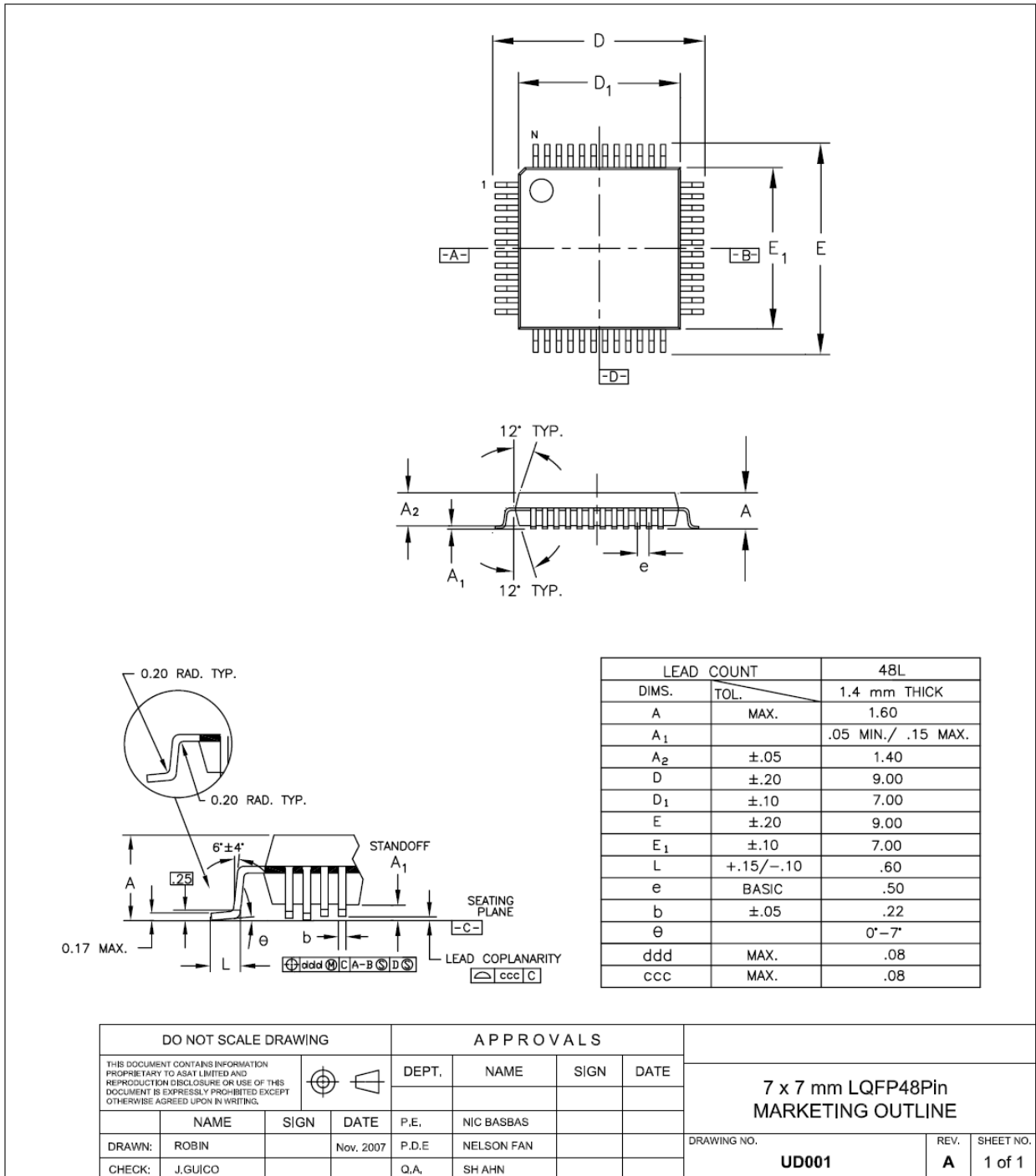
7 Typical Application



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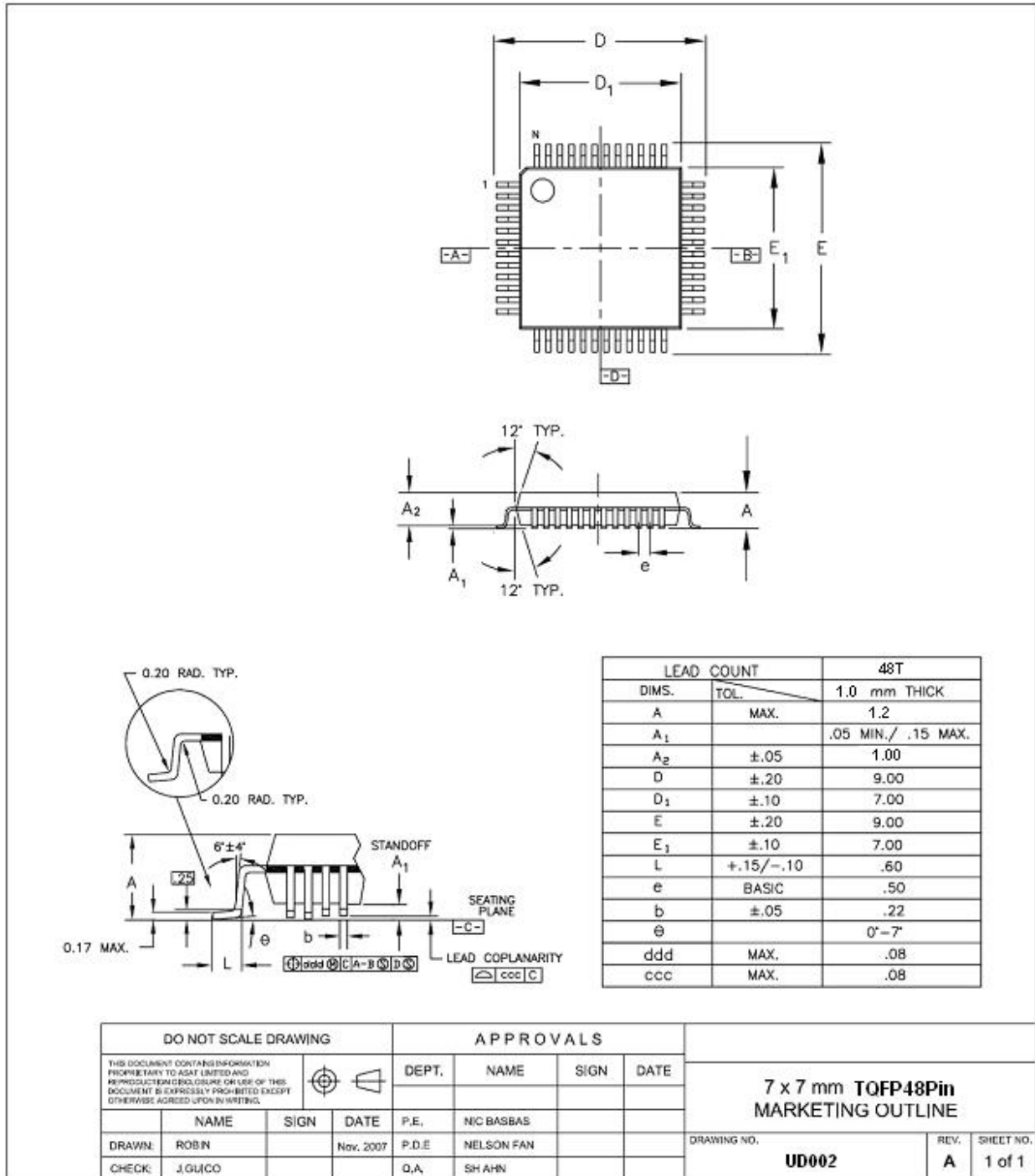
8 Mechanical Dimensions

8.1 LQFP 48-Pin UD6810 Package Outline Dimension



UD6810 Datasheet

8.2 TQFP 48-Pin UD6810 Package Outline Dimension



DO NOT SCALE DRAWING				APPROVALS				7 x 7 mm TQFP48Pin MARKETING OUTLINE		
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