24nm 64Gb eX3 (8LC)
3V NAND Flash Memory Data Sheet
(x8 TSOP)

Preliminary Version
Rev 1.0

January 24, 2011

Part Number: SDTNPNAHEM-008G

Proprietary and Confidential

For memory capacity, 1 megabyte (MB) = 1 million bytes, and 1 gigabyte (GB) = 1 billion bytes. Some of the listed capacity is used for formatting and other functions, and thus is not available for data storage.

Revision History

Version	Revision	Date	Changes
Preliminary	1.0	01/24/2011	Initial release.

Table of Contents

1. Device Overview

1.1 Description

The 64Gb eX3 (8LC) CMOS NAND E2PROM is a 3.3V NAND Electrically Erasable and Programmable Read-Only Memory with 3-bit per cell organized as (8192 + 1024) bytes × (512 + 4) logical pages × 2084 blocks or (16,384 + 2048) bytes × (256 + 2) physical pages × 2084 blocks.

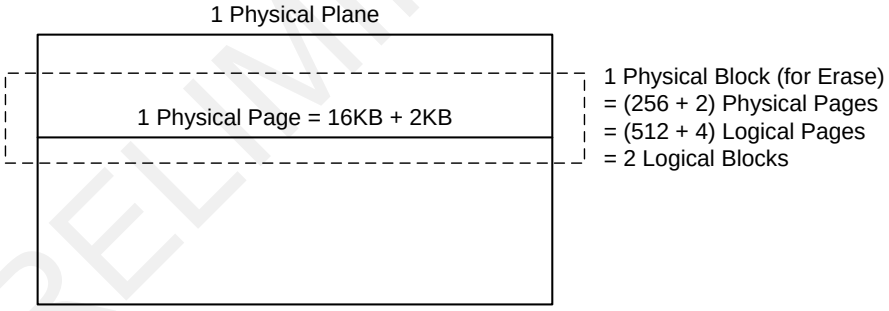
The device has two 9216-byte static registers that allow program and read data to be transferred between the register and the memory cell array in 9216-byte increments. Since there are two logical planes within one physical plane, each physical page is divided into two logical pages (even and odd). See Figure 1.

During a Program operation, data must be loaded separately into both sets of registers. Corresponding even and odd pages from the same physical block are programmed simultaneously. No partial page 8LC programming is allowed. Similarly, in a Page Read operation, both of the even and odd pages are selected and read at the same time. In an Erase operation, both of the even and odd logical blocks are selected for erase simultaneously.

The device is a serial-type memory device, which utilizes the I/O pins for both address and data input/output, as well as for command inputs. The Erase and Program operations are automatically executed, making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras, and other systems that require high-density non-volatile memory data storage.

In subsequent sections of this data sheet, all descriptions refer to the logical view (except as noted). For example, Multi-Plane operations refer to operations on two logical planes.

Physical View of Memory Array



Logical View of Memory Array

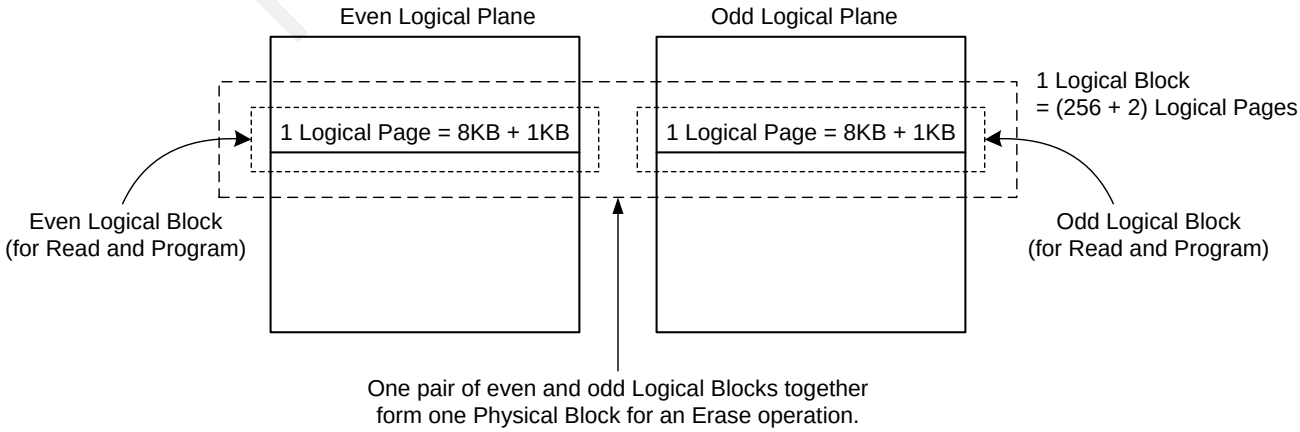


Figure 1: Physical View vs. Logical View of Memory Array

1.2 Features

Feature	64Gb eX3 (8LC)
Organization:	
Memory Cell Array	9216 x 8 x 516 pages x 2084 blocks (logical), or 18,432 x 8 x 258 pages x 2084 blocks (physical)
Register	9216 x 8 x 2
Number of Planes	2 logical planes, 1 physical plane
Block Size	(4M + 512K) bytes
Page Size	9216 bytes (logical), 18,432 bytes (physical)
Number of Pages per Block	516 (logical), 258 (physical)
Modes	ID Read, Status Read, Single-Plane Read, Multi-Plane Read, Multi-Plane Program, Multi-Plane Block Erase, SLC Read, SLC Program, SLC Erase, Dynamic Read, Multi-Plane Copy, Reset
Mode Control	Serial Input / Output, Command Control
Number of Valid Blocks	Min 1956 blocks; Max 2084 blocks
Power Supply	VCC = 2.7 V to 3.6 V
Access Time	Cell Array to Register: 220 µs max Serial Read Cycle: 25 ns min
Program / Erase Time	Single-Plane Program: 800 / 3400 / 7600 µs typ. (1^{st} / 2^{nd} / 3^{rd} cycle) Single Block Erase: 5 ms / block typ.
Operating Current	Read (25 ns cycle): 35 mA max Program (avg.): 35 mA max Erase (avg.): 35 mA max Standby: 100 µA max
Package	TSOP

1.3 Pin Functions / Pin Assignments

1.3.1 Pin Functions

This serial access memory device makes use of timesharing for input of address information.

Pin Name	Type	Description
CEn	**Input**	Chip Enable: The device goes into a low-power Standby mode when CEn goes High while the device is in Ready state. The CEn signal is ignored when the device is in Busy state (RY/BYn = L), such as during Program, Erase, or Read operations, and does not enter Standby mode even if the CEn input goes High.
WEn	**Input**	Write Enable: The WEn signal is used to control the acquisition of data from the I/O port.
REn	**Input**	Read Enable: The REn signal controls serial data output. Data is available tREA after the falling edge of REn. The internal column address counter is also incremented (Address = Address + 1) on this falling edge.
CLE	**Input**	Command Latch Enable: The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WEn signal while CLE is High.
ALE	**Input**	Address Latch Enable: The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge the WEn signal while ALE is High.
WPn	**Input**	Write Protect: The WPn signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when WPn is Low. This signal is usually used for protecting the data during the power-on/off sequence, when input signals are invalid.
RY/BYn = R/Bn	**Output**	Ready/Busy: The RY/BYn output signal is used to indicate the operating condition of the device. The RY/BYn signal is in Busy state (RY/BYn = L) during Program, Erase, and Read operations, and it returns to Ready state (RY/BYn = H) after completion of the operation. The output buffer for this pin is an open drain and this pin must be pulled up to Vcc with an appropriate resistor.
VCC	**Supply**	Power Supply, 2.7 to 3.6V
VSS	**Supply**	Ground
I/O0 to I/O7	**I/O**	I/O Ports: The I/O0 to I/O7 pins are used as a port for transferring address, command, and input/output data to and from the device.
NC		Do Not Connect

1.3.2 TSOP 48-Pin Assignment

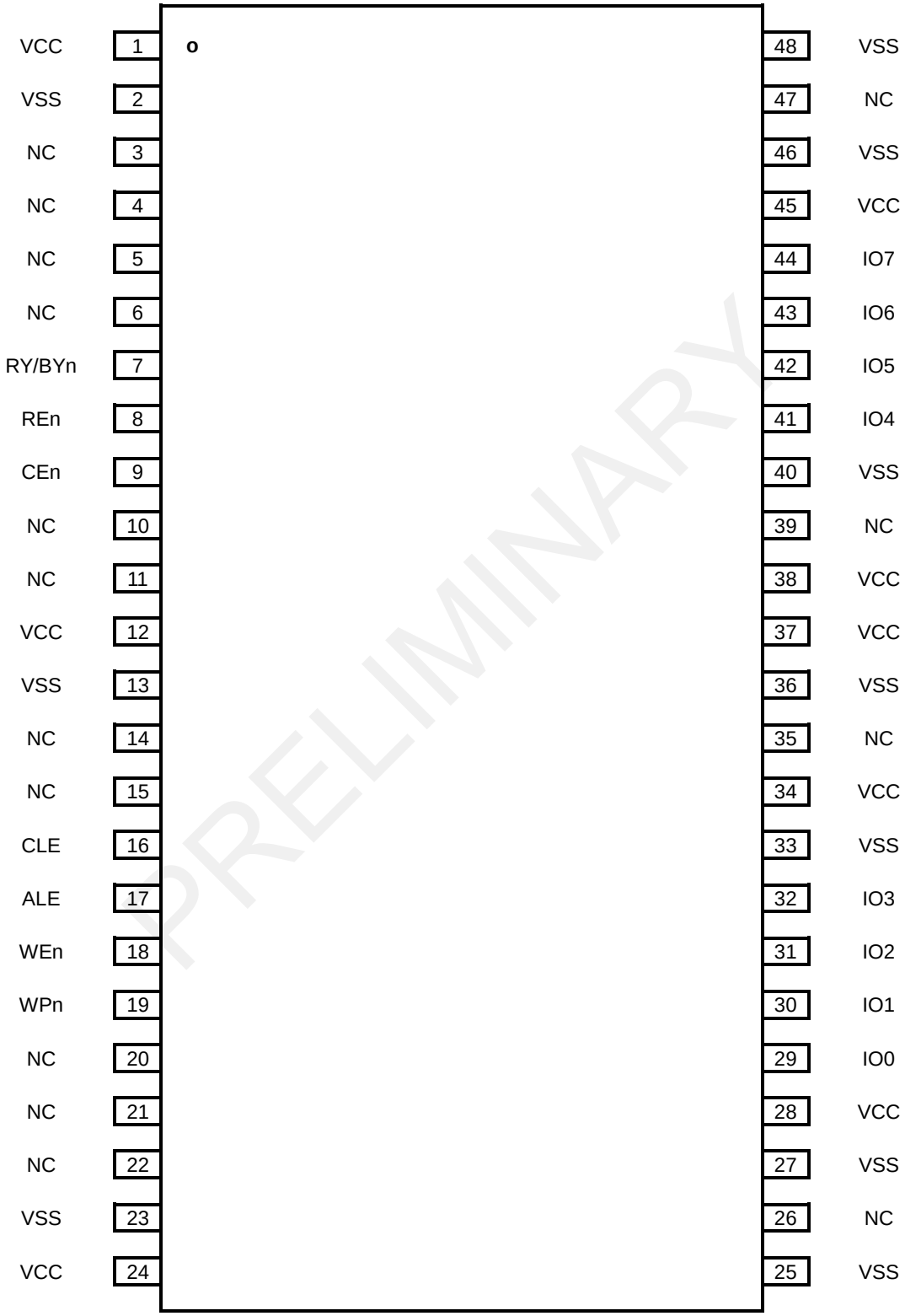
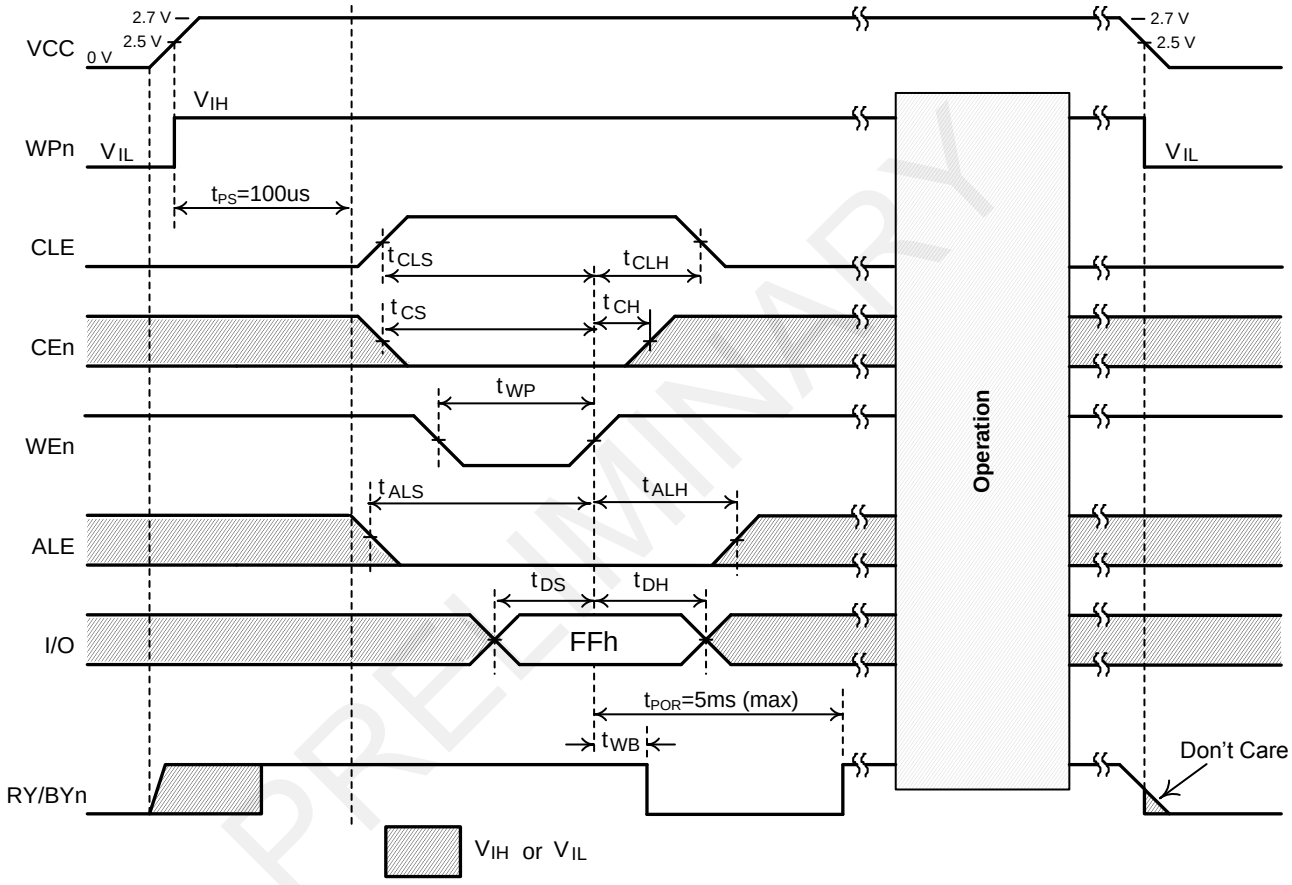


Figure 2: TSOP 48-Pin Assignment (Top View)

1.3.3 Power-On/Off Sequence

The device is designed to offer protection from any inadvertent Program or Erase commands issued during power transitions. An FFh Reset command must be issued after power up to initialize the device. During the FFh Reset Busy period, the device consumes a maximum current of 35mA (I_{CCO0}).

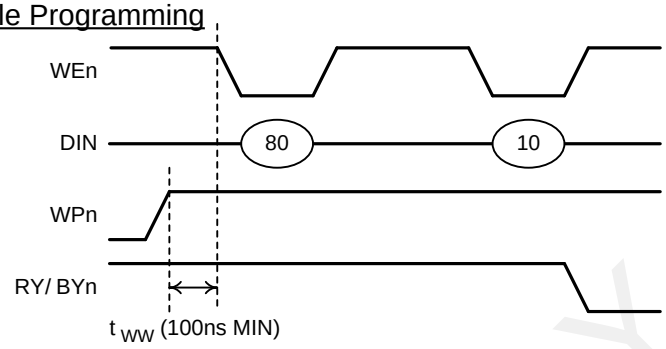
To further provide a hardware protection against data corruption, it is highly recommended that the WPn signal be kept Low during the initial power-on and power-off sequence, as shown in the diagram below.



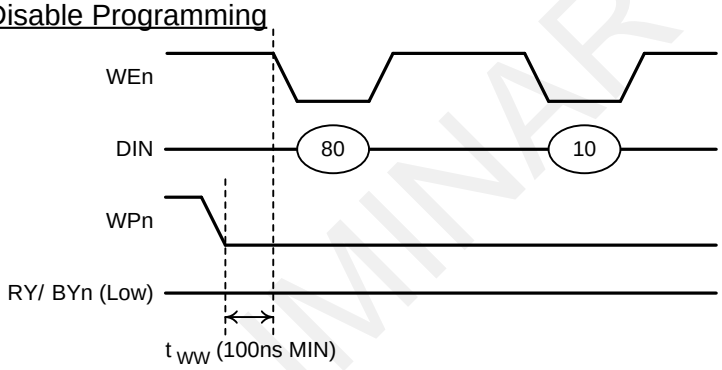
1.3.4 WPn Signal

Erase and Program operations are automatically reset when the WPn signal goes Low. The operations are enabled and disabled, as follows:

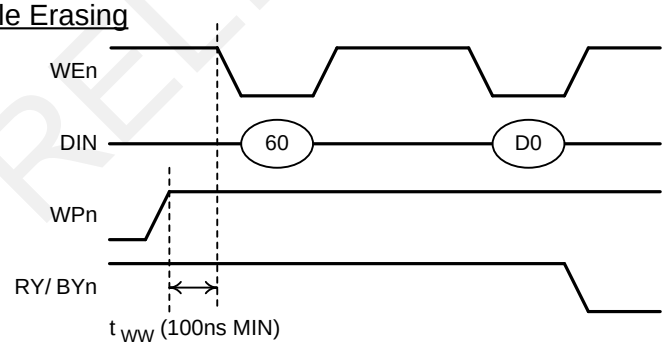
Enable Programming



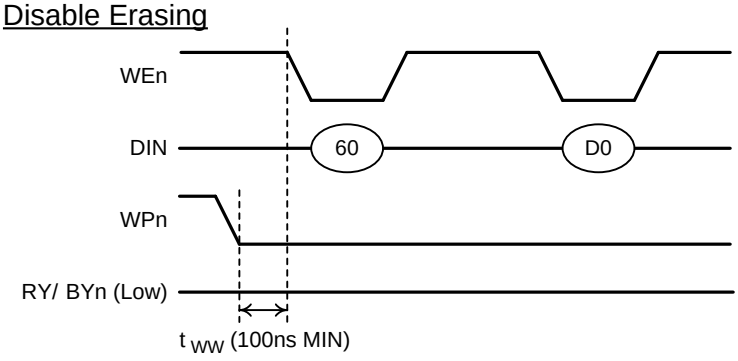
Disable Programming



Enable Erasing



Disable Erasing



1.4 Absolute Maximum Ratings

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	–0.6 to 4.6	V
V_{IN}	Input Voltage	–0.6 to 4.6	V
$V_{I/O}$	Input/Output Voltage	–0.6 to V_{CC} + 0.3 (≤ 4.6)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STG}	Storage Temperature	–55 to 150	°C

Note: Permanent device damage might occur if these Absolute Maximum Ratings are exceeded. Functional operations should be restricted to the Recommended Operating Conditions in sections 1.7 through 1.11. Exposure to Absolute Maximum Rating conditions for extended periods might affect reliability and functionality of the device.

1.5 Capacitance

(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
C_{IN} *	Input	V_{IN} = 0 V	---	4	8	pF
C_{OUT} *	Output	V_{OUT} = 0 V	---	4	8	pF

* This parameter is periodically sampled and is not tested for every device.

1.6 Valid Blocks

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Total number of Valid Blocks	1956	---	2084	Blocks

NOTE:

The device occasionally contains unusable blocks. Refer to Application Note 6.4 in this document.

The specification for the minimum number of valid blocks is applicable at time of shipment.

1.7 Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	---	3.6	V
V_{IH}	High-Level Input Voltage 2.7 V ≤ V_{CC} ≤ 3.6 V	0.8 x V_{CC}	---	V_{CC} + 0.3	V
V_{IL}	Low-Level Input Voltage 2.7 V ≤ V_{CC} ≤ 3.6 V	–0.3 *	---	0.2 x V_{CC}	V

* –2 V (pulse width less than 20 ns)

1.8 DC Characteristics

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	–	–	±10	µA
I_{CCO0}	Power On Reset Current	FFh command input after Power On	–	–	35	mA
I_{CCO1}	Serial Read Current	CEn = V_{IL} , I_{OUT} = 0 mA, tcycle = 25 ns	–	–	35	mA
I_{CCO2}	Programming Current	---	–	–	35	mA
I_{CCO3}	Erasing Current	---	–	–	35	mA
I_{CCS}	Standby Current	CEn = V_{CC} – 0.2 V, WPn = 0 V/ V_{CC}	–	–	100	µA
V_{OH}	High-Level Output Voltage	I_{OH} = – 0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	–	–	V
V_{OL}	Low-Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	–	–	0.4	V
I_{OL} (RY/BYn)	Output Current of RY/BYn Pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	–	8	–	mA

1.9 AC Characteristics and Recommended Operating Conditions

(Ta = 0 to 70°C, VCC = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCLS	CLE Setup Time	15	–	ns
tCLS2	CLE Setup Time	30	–	ns
tCLH	CLE Hold Time	5	–	ns
tCS	CE Setup Time	20	–	ns
tCS2	CE Setup Time	20	–	ns
tCH	CE Hold Time	5	–	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	15	–	ns
tALH	ALE Hold Time	5	–	ns
tDS	Data Setup Time	10	–	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	WE High Hold Time	10	–	ns
tWHWP	Preconditioning WE High Hold Time	100	–	ns
tWHW *	WE High Hold Time from final address to first data	300	–	ns
tWW	WP High to WE Low	100	–	ns
tRR	Ready to RE Falling Edge	20	–	ns
tRW	Ready to WE Falling Edge	0	–	ns
tRP	Read Pulse Width	12	–	ns
tRC	Read Cycle Time	25	–	ns
tREA	RE Access Time	–	20	ns
tCR	CE Low to RE Low	10	–	ns
tCLR	CLE Low to RE Low	10	–	ns
tAR	ALE Low to RE Low	10	–	ns
tRHOH	Data Output Hold Time from RE High	25	–	ns
tRLOH	Data Output Hold Time from RE Low	5	–	ns
tCHOH	Data Output Hold Time from CE High	10	–	ns
tRHZ	RE High to Output High Impedance	–	60	ns
tCHZ	CE High to Output High Impedance	–	30	ns
tCLHZ	CLE High to Output High Impedance	–	30	ns
tREH	RE High Hold Time	10	–	ns
tIR	Output High Impedance to RE Falling Edge	–	0	ns
tRHW	RE High to WE Low	30	–	ns
tWHC	WE High to CE Low	30	–	ns
tWHR	WE High to RE Low (Register Read)	300	–	ns
tWHRS	WE High to RE Low (Status Read)	180	–	ns
tR1	Data Read Time 1	–	120	µs
tR2	Data Read Time 2	–	150	µs
tR3	Data Read Time 3	–	120	µs
tRS	SLC Data Read Time	–	50	µs
tWB	WE High to Busy	–	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	10/20/30/500	µs

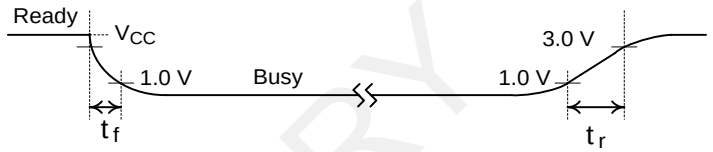
* tWHW is for 80h / 85h command sequence only. It is the time from the WEn rising edge of the fifth address cycle to the WEn falling edge of the first data or command cycle.

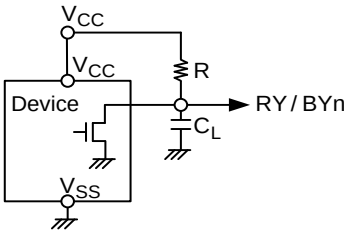
1.10 AC Test Conditions

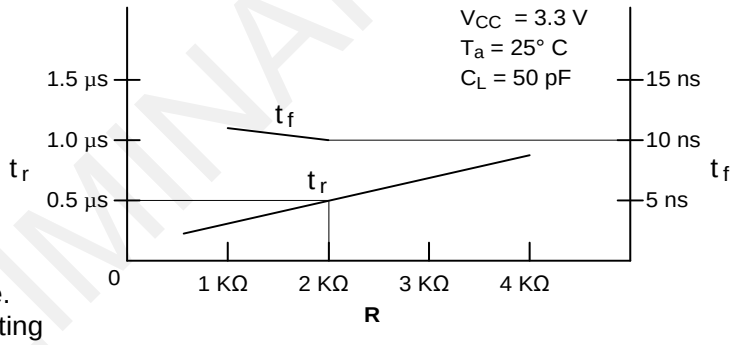
PARAMETER	CONDITION
	2.7 V ≤ V_{CC} ≤ 3.6 V
Input Level	0V to V_{CC}
Input Pulse Rise and Fall Time	3ns
Input Comparison Level	1/2 V_{CC}
Output Data Comparison Level	1/2 V_{CC}
Output Load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/BYn pin.

A pull-up resistor must be used for termination, because the RY/BYn buffer consists of an open drain circuit.







This data might vary from device to device. Using this data as a reference when selecting a resistor value is recommended.

1.11 Programming and Erasing Characteristics

(Ta = 0 to 70°C, VCC = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG1}	Programming Time 1	–	800	1200	µs	
t_{PROG2}	Programming Time 2	–	3400	5000	µs	
t_{PROG3}	Programming Time 3	–	7600	11000	µs	
t_{PROGS}	SLC Programming Time	–	400	1000	µs	
t_{DCBSY1}	Data Cache Busy Time in Write Cache (following 11h or 1Ah)	–	10	–	µs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	–	–	3000	µs	(1)
N	Number of Partial Program Cycles in the Same Page	–	–	0	cycle	(2)
t_{BERASE}	Block Erase Time	–	5	10	ms	
$t_{BERASES}$	SLC Block Erase Time	–	5	10	ms	

(1) $t_{DCBSYW2}$ depends on the timing between internal programming time and data-in time.
(2) This device does not support partial page programming.

2. Address Assignment

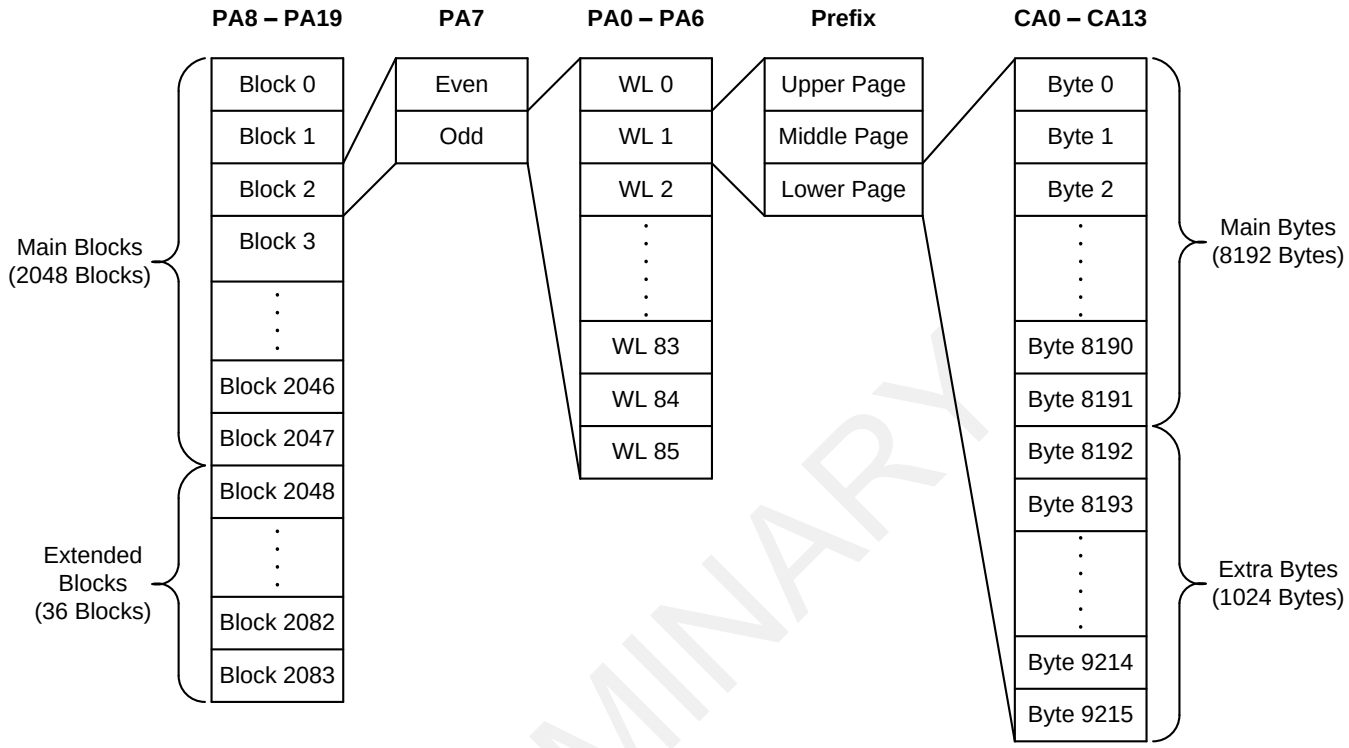


Table 1: Addressing

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First Cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second Cycle	X	X	CA13	CA12	CA11	CA10	CA9	CA8
Third Cycle	X	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth Cycle	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7
Fifth Cycle	X	X	X	PA19	PA18	PA17	PA16	PA15

CA0 to CA13 : Column Address

PA0 to PA6 : Physical WL Address (1)

PA7: Logical Address selecting between even and odd logical planes

PA8 to PA19 : Physical Block Address (2)

Notes:

(1) Only WL0 to WL85 are valid WL addresses. Corresponding even and odd WL pairs are selected together for Program and Read operations.

(2) Only Block0 to Block2083 are valid physical block addresses.

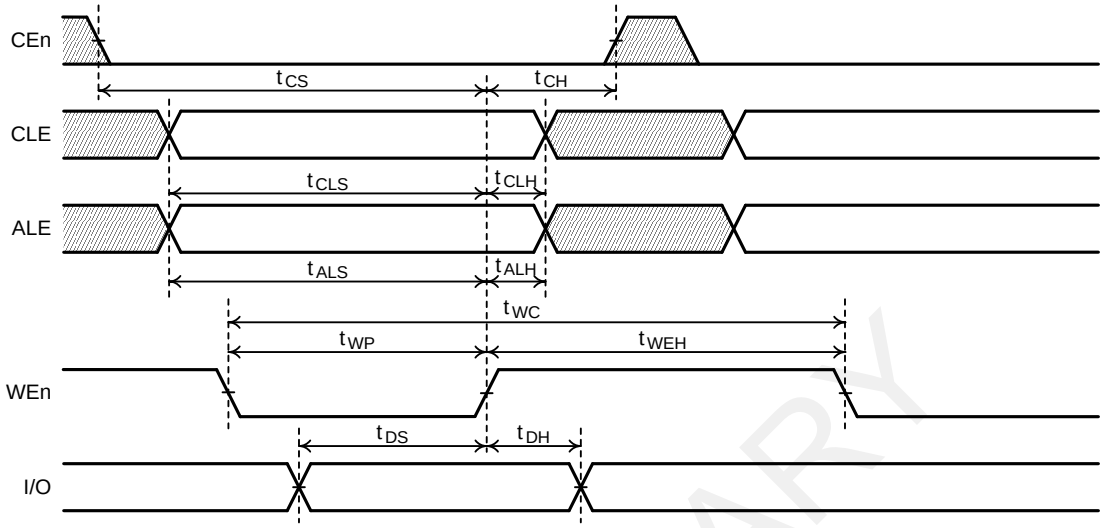
(3) Lower / Middle / Upper Pages are selected by the Prefix command.

(4) SLC addressing is the same as 8LC addressing.

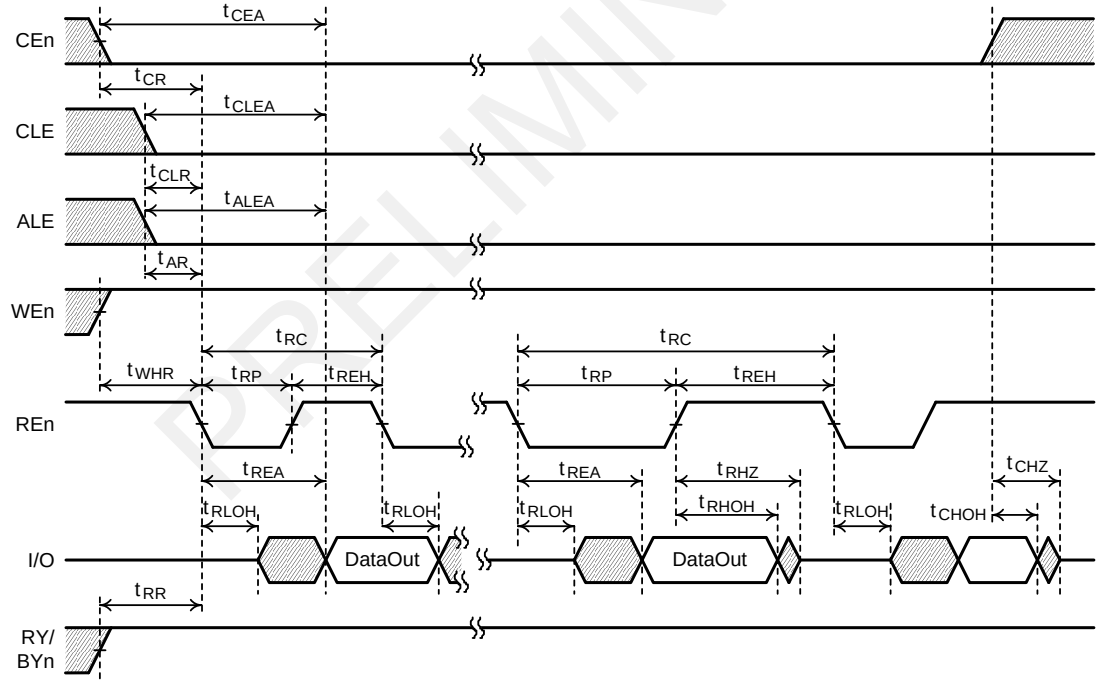
(5) X = Don't Care.

3. Timing Diagrams

3.1 Write Timing



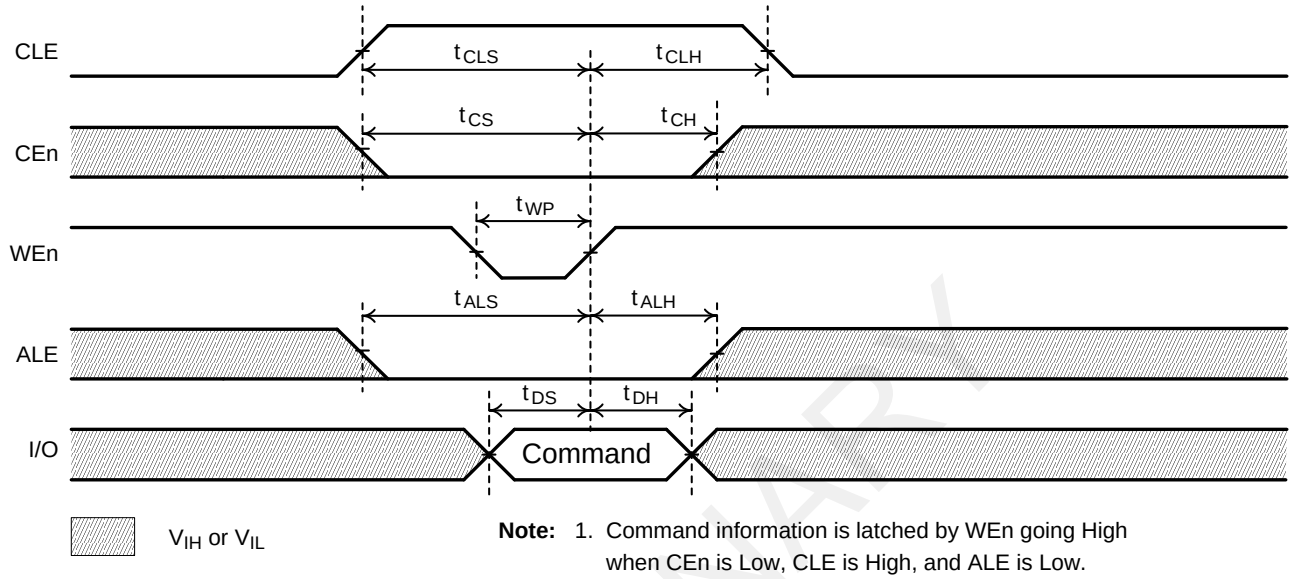
3.2 Read Timing



Notes:

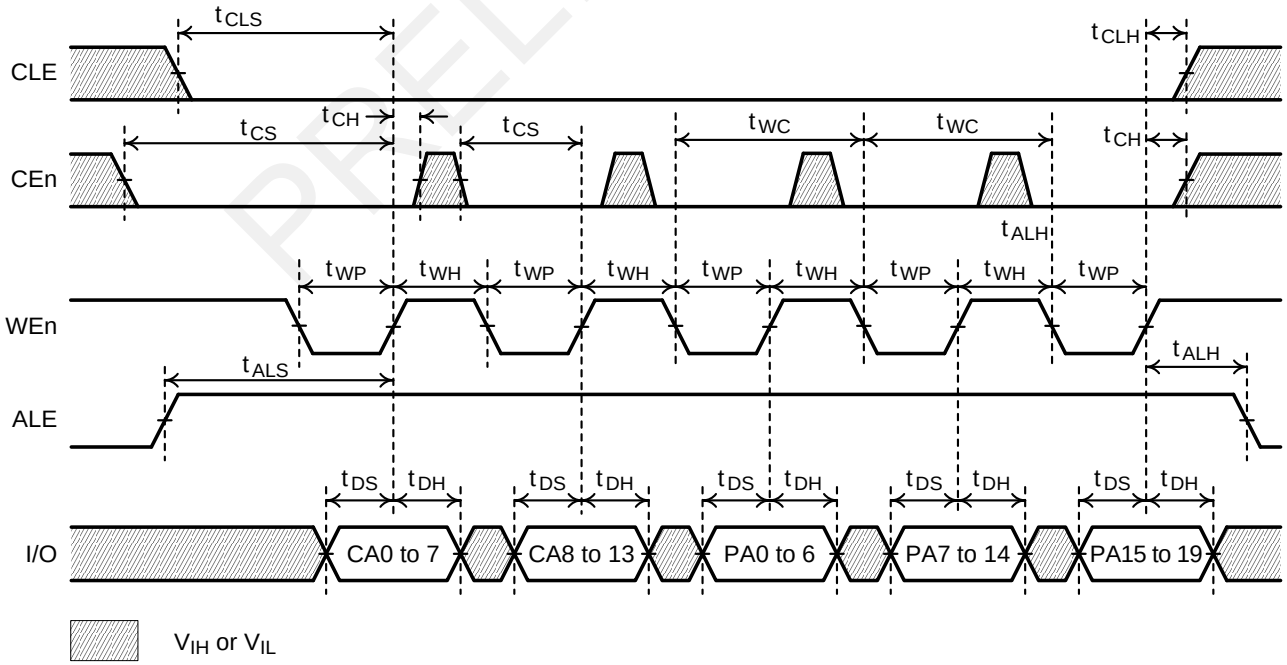
- Hold time from REn rising edge is determined by the shorter one of either tRHOH or tREH + tRLOH.
- When tREH is long, output buffers are disabled by REn=High, and the hold time of data output depends on tRHOH (30 ns MIN). On this condition, waveforms look like normal serial read mode. (For instance, when tREH = 30ns, it is tRHOH = 30ns.)
- When tREH is short, output buffers are not disabled by REn=High, and the hold time of data output depends on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, CEn, or the falling edge of WEn, and waveforms look like Extended Data Output Mode. (For instance, when tREH = 10ns, it is tRHOH = tREH + tRLOH = 15ns.)

3.3 Command Input Cycle Timing

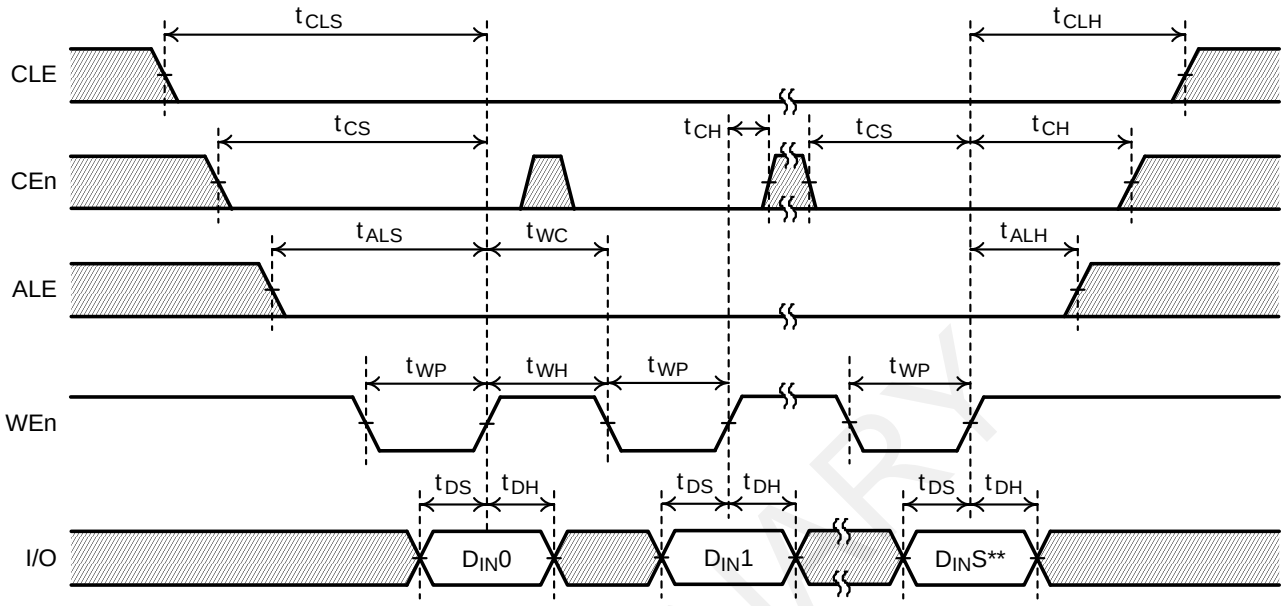


Note: 1. Command information is latched by WEn going High when CEn is Low, CLE is High, and ALE is Low.

3.4 Address Input Cycle Timing



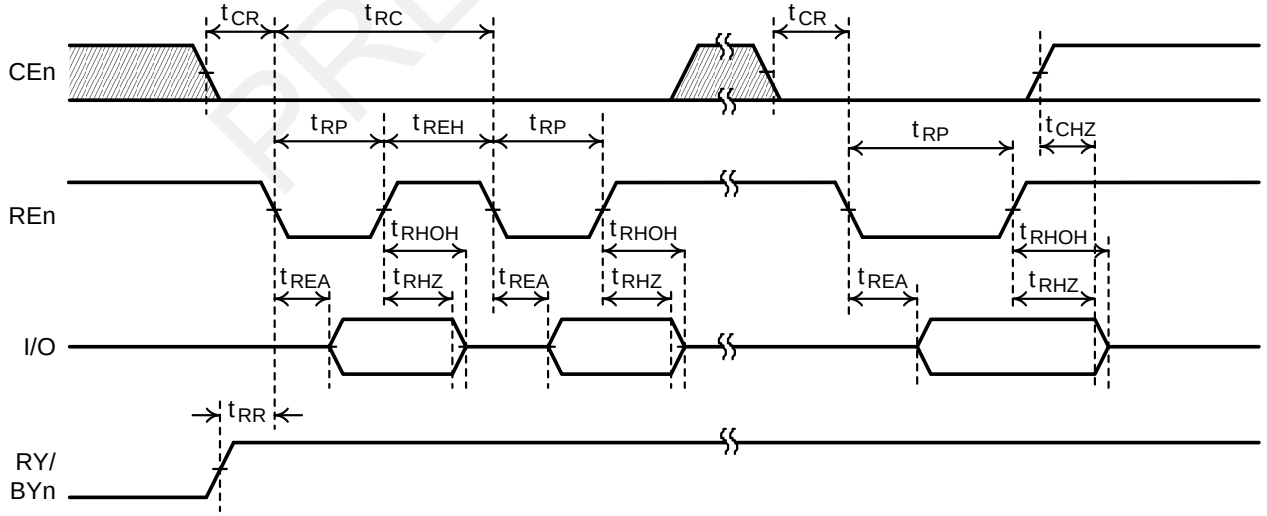
3.5 Data Input Cycle Timing



V_{IH} or V_{IL}

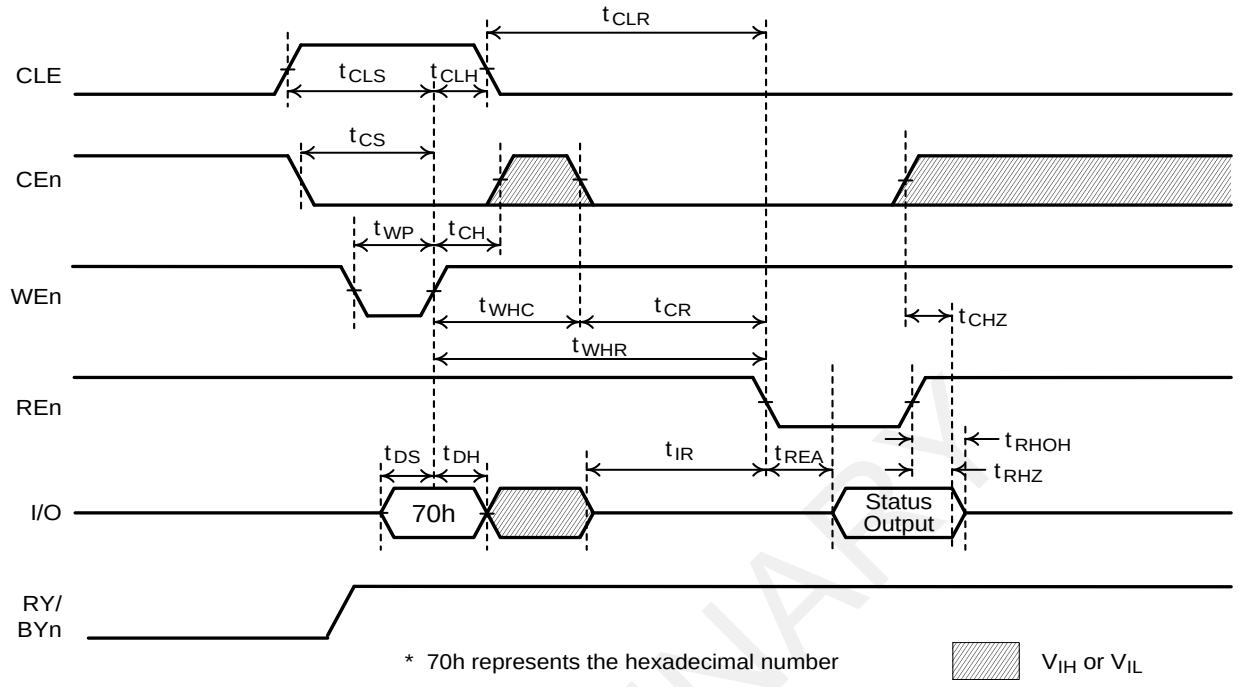
** S = 9215

3.6 Serial Read Cycle Timing

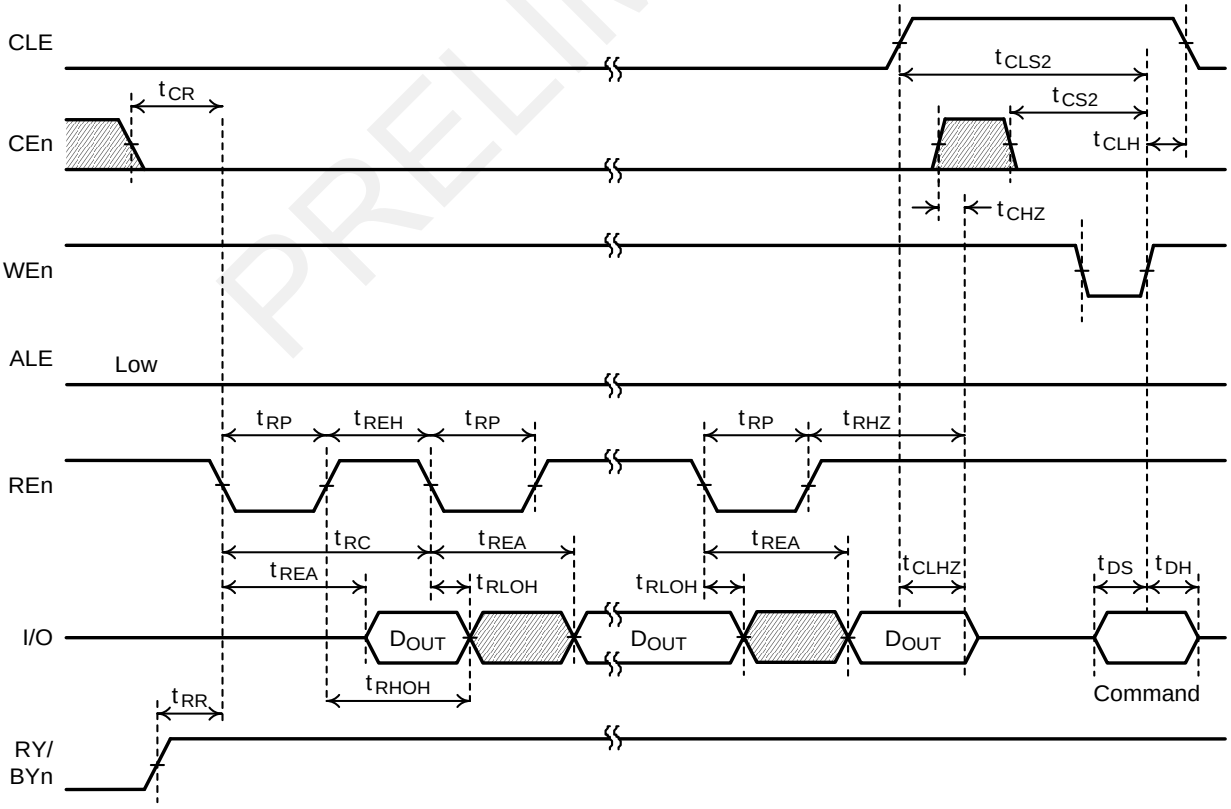


V_{IH} or V_{IL}

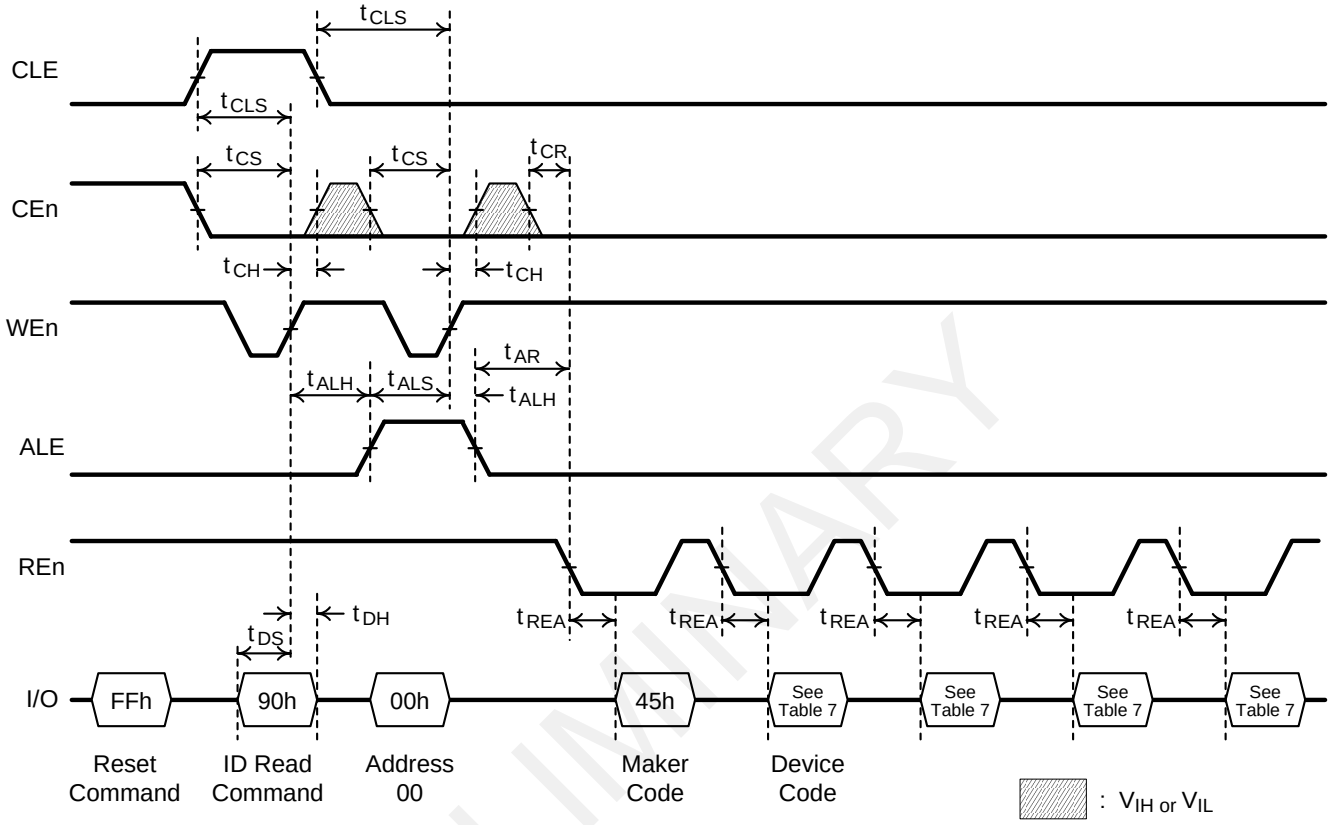
3.7 Status Read Cycle Timing



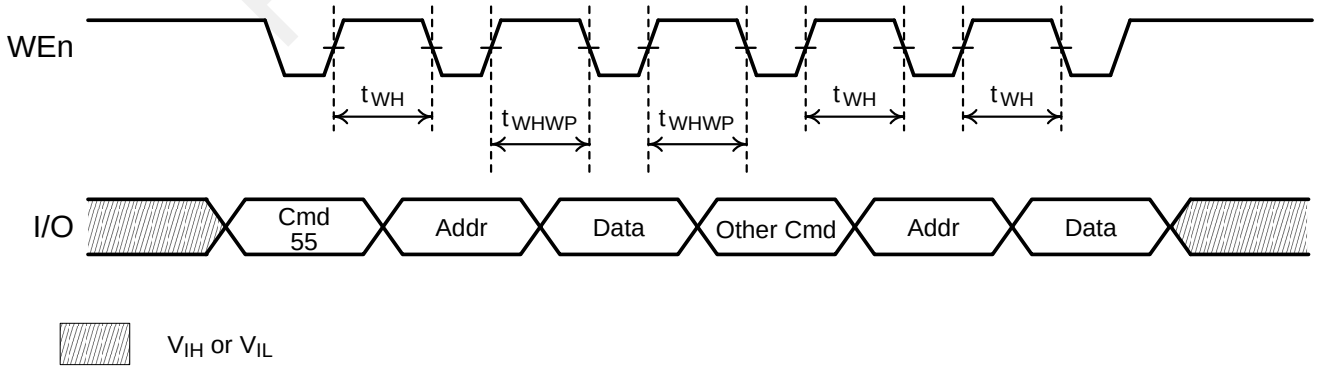
3.8 Data Output Timing



3.9 ID Read Operation Timing



3.10 Preconditioning Mode Timing



4. Operation Mode: Logic and Command Tables

4.1 Logic Table

Address input, command input, and data input/output are controlled by the CLE, ALE, CEn, WEn, REn, and WPn signals, as shown in Table 2. Operation modes such as Program, Erase, Read, and Reset are controlled by command operations shown in Table 3.

Table 2: Logic Table

	CLE	ALE	CEn	WEn	REn	WPn (*1)
Command Input	H	L	L		H	*
Data Input	L	L	L		H	H
Address Input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V / V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: See the "WPn Signal" section for details regarding Program and Erase operations when WPn goes Low.

*2: If CEn is Low during read busy, WEn and REn must be held High to avoid unintended command / address input to the device or read to the device. Reset or Status Read commands can be input during Read (Busy).

4.2 Command Table

Table 3: Command Table (HEX)

Command (See Notes 1 and 2)	Code	Acceptable while Busy	Preconditioning Mode Command
Read Address Input	00		
Prefix for Lower Page Select (for Read and Program)	01		
Prefix for Middle Page Select (for Read and Program)	02		
Prefix for Upper Page Select (for Read and Program)	03		
Register Read Address Input	05		
First Program Cycle	09		
Second Program Cycle	0D		
Third Program Cycle	10		
Program (Dummy)	11		
Cache Program	15		
Multi-Page Data Load for Program	1A		
Read	30		
Cache Read With Address Change	3C		
Cache Read	3F		
Preconditioning	55		•
Preconditioning Mode Entry	5C – C5		•
Prefix for Dynamic Read	5D		•
Block Address Input	60		
Bad Column Address Read Out	69		•
Status Read	70	•	
Address Input for Data Load	80		
Address Input for Data Load without Reset	85		
ID Read	90		
Prefix for SLC Mode (for Read, Program, and Erase)	A2		
Block Erase	D0		
Register Read	E0		
Reset	FF	•	

Notes:
1. Input of a command other than those specified in Table 3 is prohibited. Stored data can be corrupted if an unknown command is entered during the command cycle.
2. During the Busy state, do not input any command except 70h or FFh.

Table 4: Read Mode Operation States for Read mode, when tREH is long

	CLE	ALE	CEn	WEn	REn	I/O0 to I/O7	Power
Output Select	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active

H: V_{IH}, L: V_{IL}

5. Device Operation

5.1 Multi-Plane Operations

Two pages, one in the even logical plane and the corresponding page in the odd logical plane, must be selected for simultaneous execution during Read or Program operations. Similarly, two blocks, one in the even logical plane and the corresponding block in the odd logical plane, must be selected for simultaneous execution during Erase operations. Single-plane 8LC operations are not allowed.

5.2 Read Operations

Three pages of data are contained in each WL address. The page numbers within one block are defined in Table 5. The selection of Lower / Middle / Upper page is achieved by using a 01h / 02h / 03h prefix. One pair of pages (one from the even plane and one from the odd plane) is selected for simultaneous Read operation.

Table 5: Page Numbering Within a Block

WL #	Lower Page		Middle Page		Upper Page	
	Even Plane	Odd Plane	Even Plane	Odd Plane	Even Plane	Odd Plane
WL0	0	258	1	259	2	260
WL1	3	261	4	262	5	263
WL2	6	264	7	265	8	266
WL3	9	267	10	268	11	269
:	:	:	:	:	:	:
WL84	252	510	253	511	254	512
WL85	255	513	256	514	257	515

5.3 Program Order

SanDisk requires the following program order (in **bold**) for programming the pages within a block. Random page program sequences are prohibited. Page data must be input and programmed three times into the page. Data from the three pages in a WL can be read out only after the third program cycle of the next WL is completed. The exception is for the last WL (WL85) of a block. Its data can be read out after the third program cycle of this WL.

The Normal (8LC) Program Data for both pages (from the even and odd planes) must be loaded into their respective registers before the actual Program command (10h or 15h). Single (logical) plane programming and partial page programming are not allowed in 8LC devices.

WL #	Page Numbers		Program Order		
	Even Plane	Odd Plane	First Program Cycle	Second Program Cycle	Third Program Cycle
WL0	0,1,2	258, 259, 260	**1**	**3**	**6**
WL1	3,4,5	261, 262, 263	**2**	**5**	**9**
WL2	6,7,8	264, 265, 266	**4**	**8**	**12**
WL3	9,10,11	267, 268, 269	**7**	**11**	**15**
WL4	12,13,14	270, 271, 272	**10**	**14**	**18**
:	:	:	**:**	**:**	**:**
WL82	246,247,248	504, 505, 506	**244**	**248**	**252**
WL83	249,250,251	507, 508, 509	**247**	**251**	**255**
WL84	252,253,254	510, 511, 512	**250**	**254**	**257**
WL85	255,256,257	513, 514, 515	**253**	**256**	**258**

5.4 SLC Mode (for Read, Program, and Erase Operations)

In addition to the Normal (8LC) mode, the device supports an SLC mode, which can be used with data that requires frequent updates, high performance, and high reliability.

After initial power-up, the device defaults to Normal mode. To operate in SLC mode, an A2h command must be added as a prefix to the Normal command for Read, Program, or Erase.

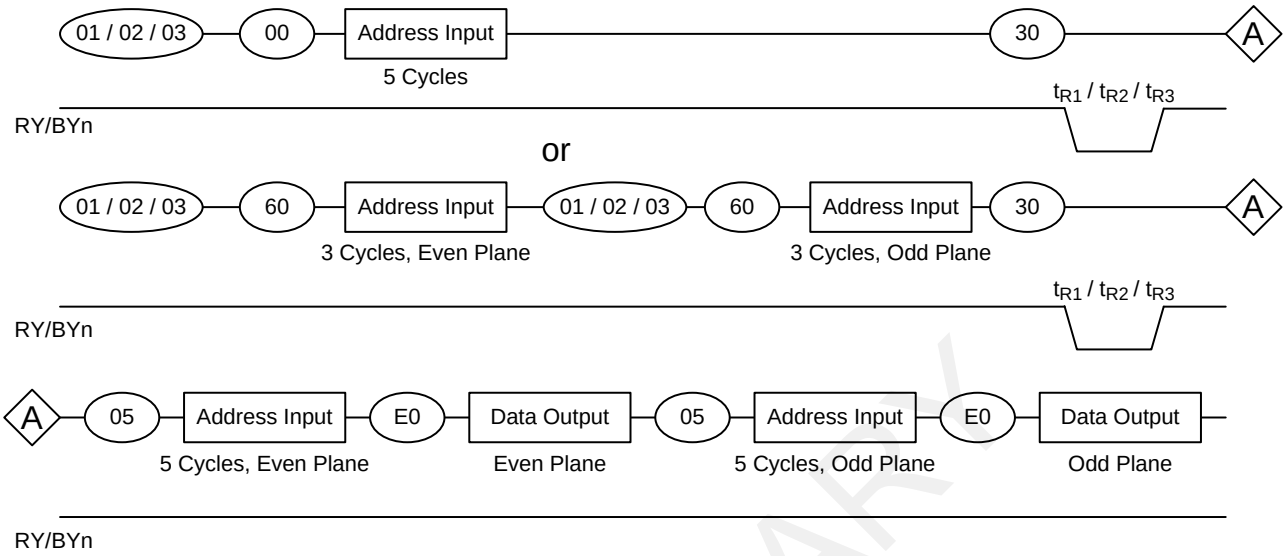
When the data in a block is programmed in one mode (Normal or SLC), the data must be read or erased using the same mode; the mode cannot be switched within a block. The SLC mode automatically resets to the Normal mode at the end of a Read, Program, or Erase operation.

A block assigned to operate in one mode (Normal or SLC) should always stay to operate in the same mode during the life of the device.

When one block is under a Normal (8LC) Program operation, the whole block has to complete programming before another block can be selected for Normal Programming. However, SLC Program, SLC/Normal Read or SLC/Normal Erase command for another block can be issued when one block is under a Normal Program operation. This restriction does not apply to a block under SLC Program operation.

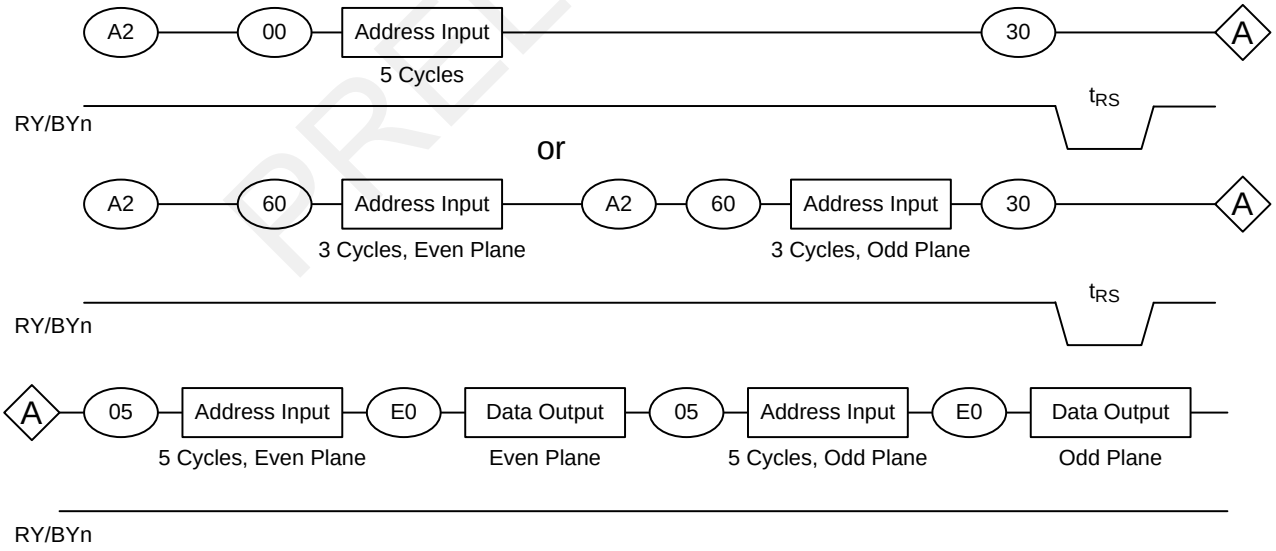
In SLC Program operations, each logical page can be partially programmed up to four times. (Each physical page can be partially programmed up to eight times.) Partial page programming is not allowed for Normal (8LC) Program operations.

5.5 Multi-Plane Page-by-Page Read Mode



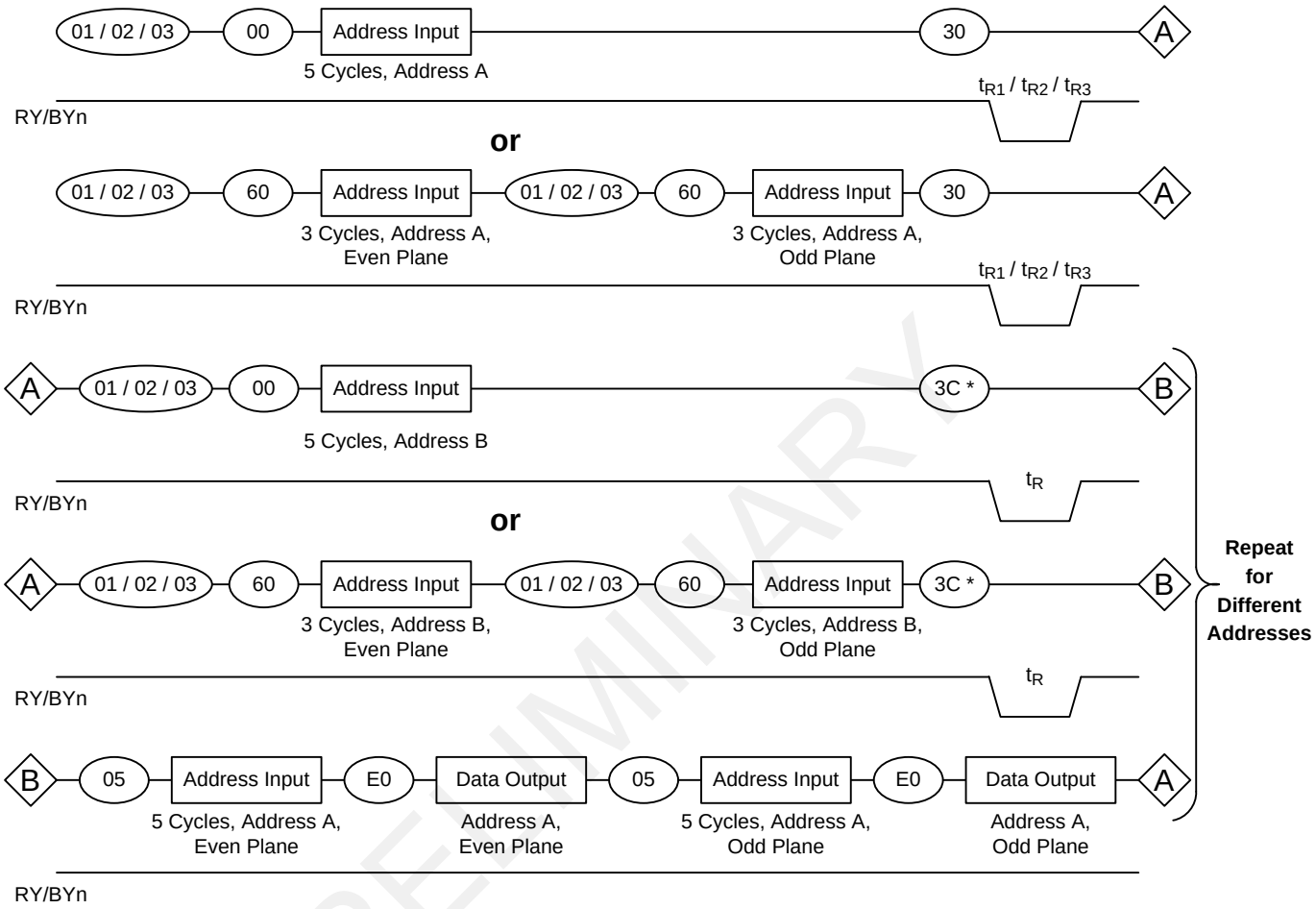
Notes: 01h / 02h / 03h = Prefix commands for Lower / Middle / Upper page.
The Lower / Middle / Upper page data can be read individually or in any order.
The sequence for Even / Odd planes can be reversed.

5.6 Multi-Plane SLC Read Mode



Notes: A2h = Prefix command for SLC mode.
The sequence for Even / Odd planes can be reversed.

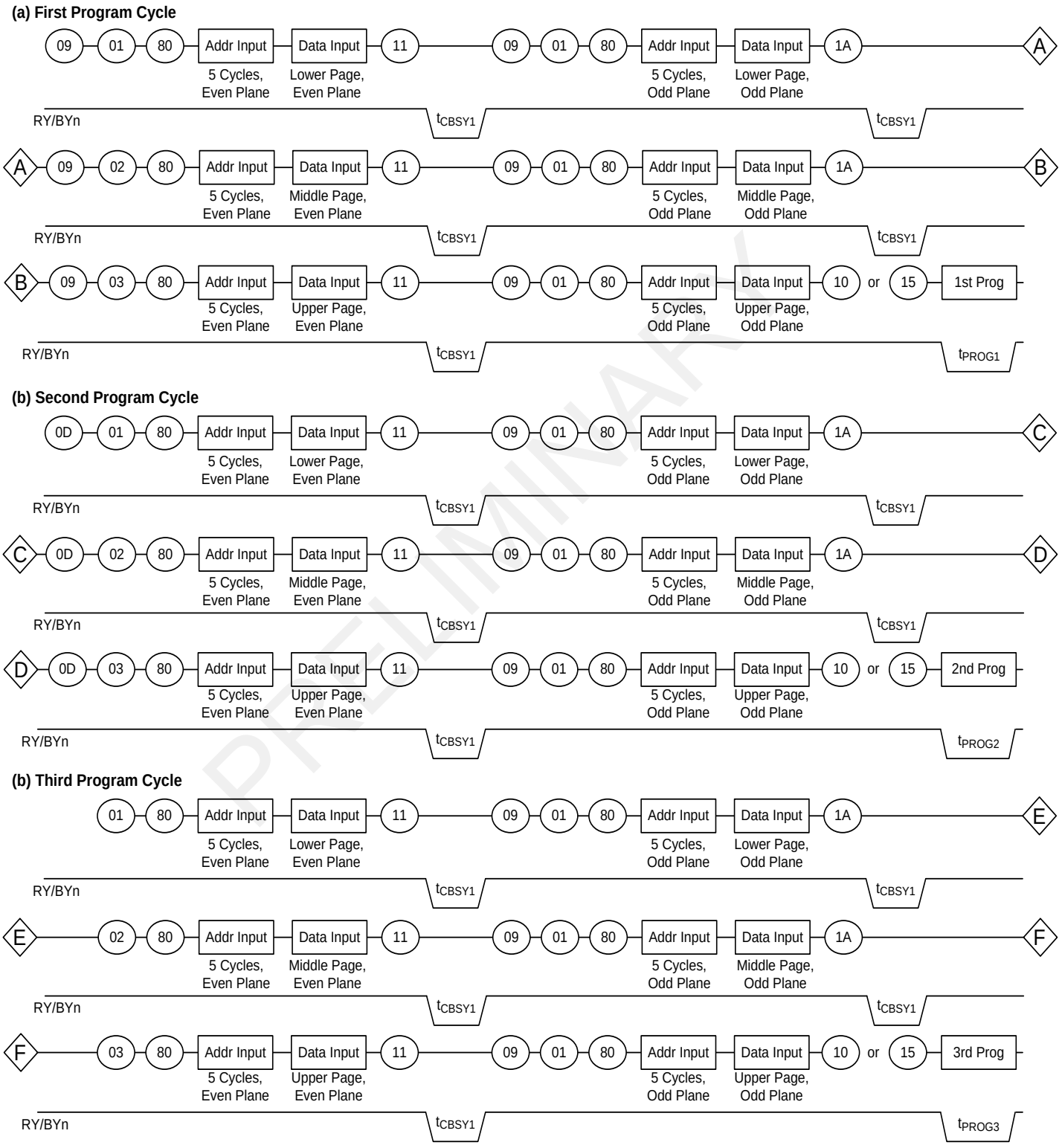
5.7 Multi-Plane Cache Read Mode



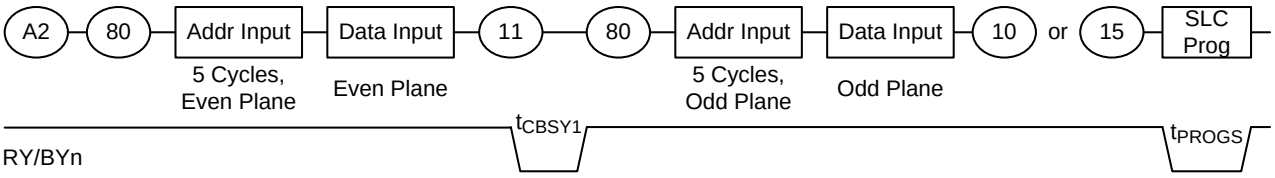
***** After the last address, terminate the Cache Read operation with a 3Fh command instead of using a 3Ch command.

5.8 Multi-Plane Program Mode

The program order defined in section 5.3 must be followed.



5.9 Multi-Plane SLC Program Mode



Notes for Sections 5.8 and 5.9:

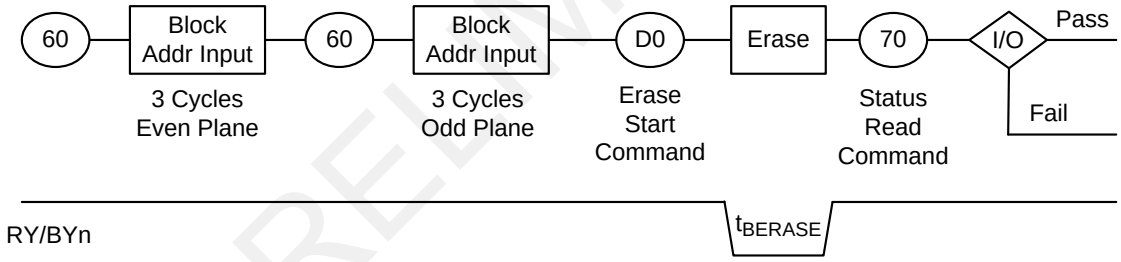
10 Program command without using write cache.

15 Program command using write cache.

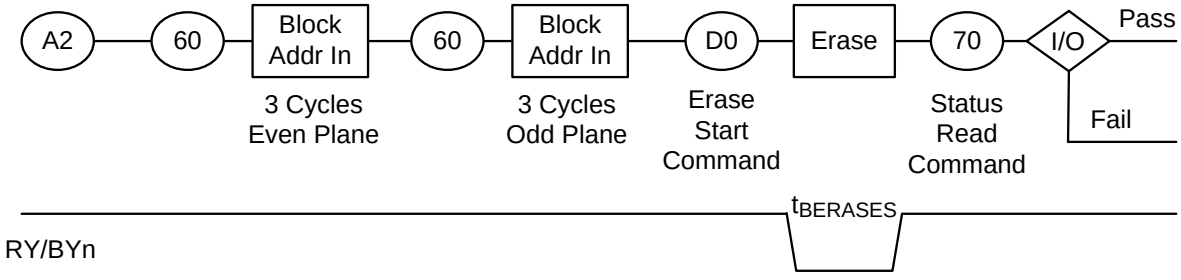
Block address must be the same for Even and Odd planes.
The sequence for Even / Odd planes can be reversed.

5.10 Multi-Plane Block Erase Mode

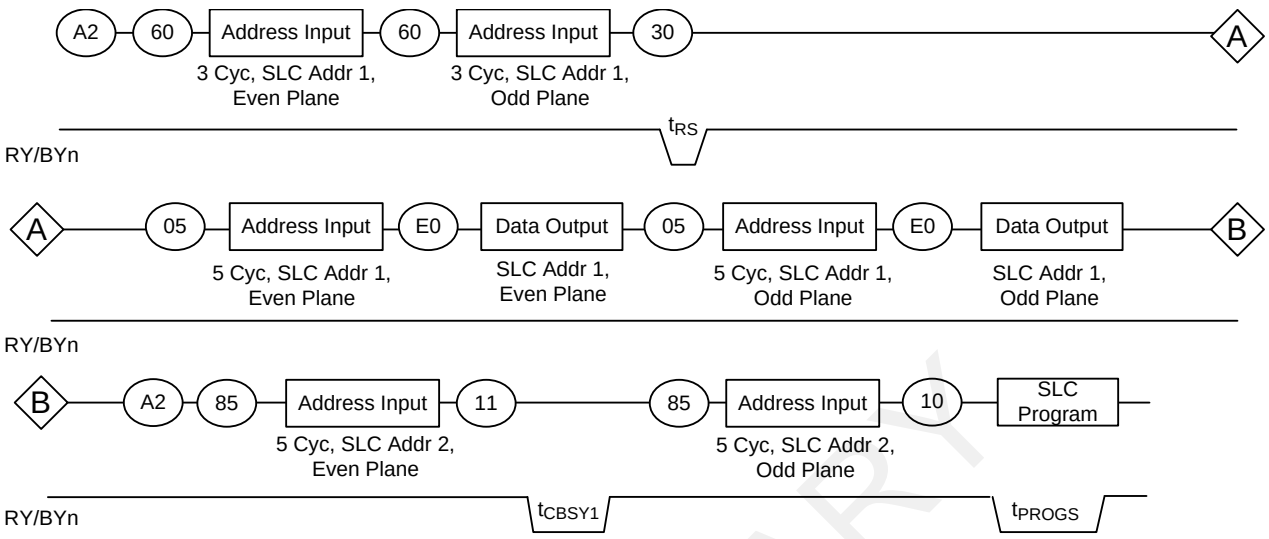
The Multi-Plane Block Erase operation starts by selecting the same block address for the Even and Odd planes before a D0h command, as in the diagram below. The device automatically executes the Erase and Verify operations, and the result can be monitored by checking the status using the 70h Status Read command.



5.11 Multi-Plane SLC Block Erase Mode



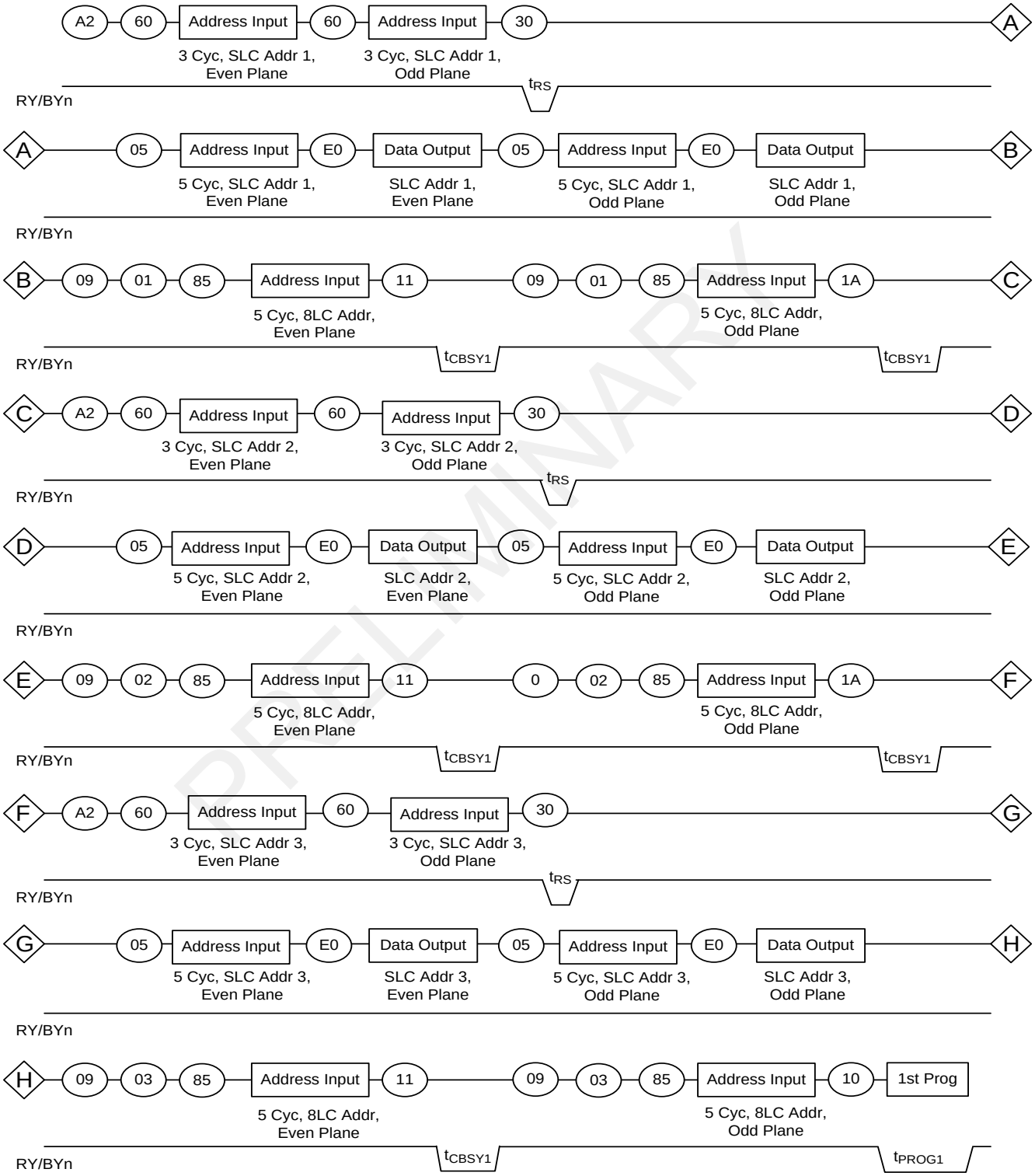
5.12 Multi-Plane Copy Mode (SLC -> SLC)



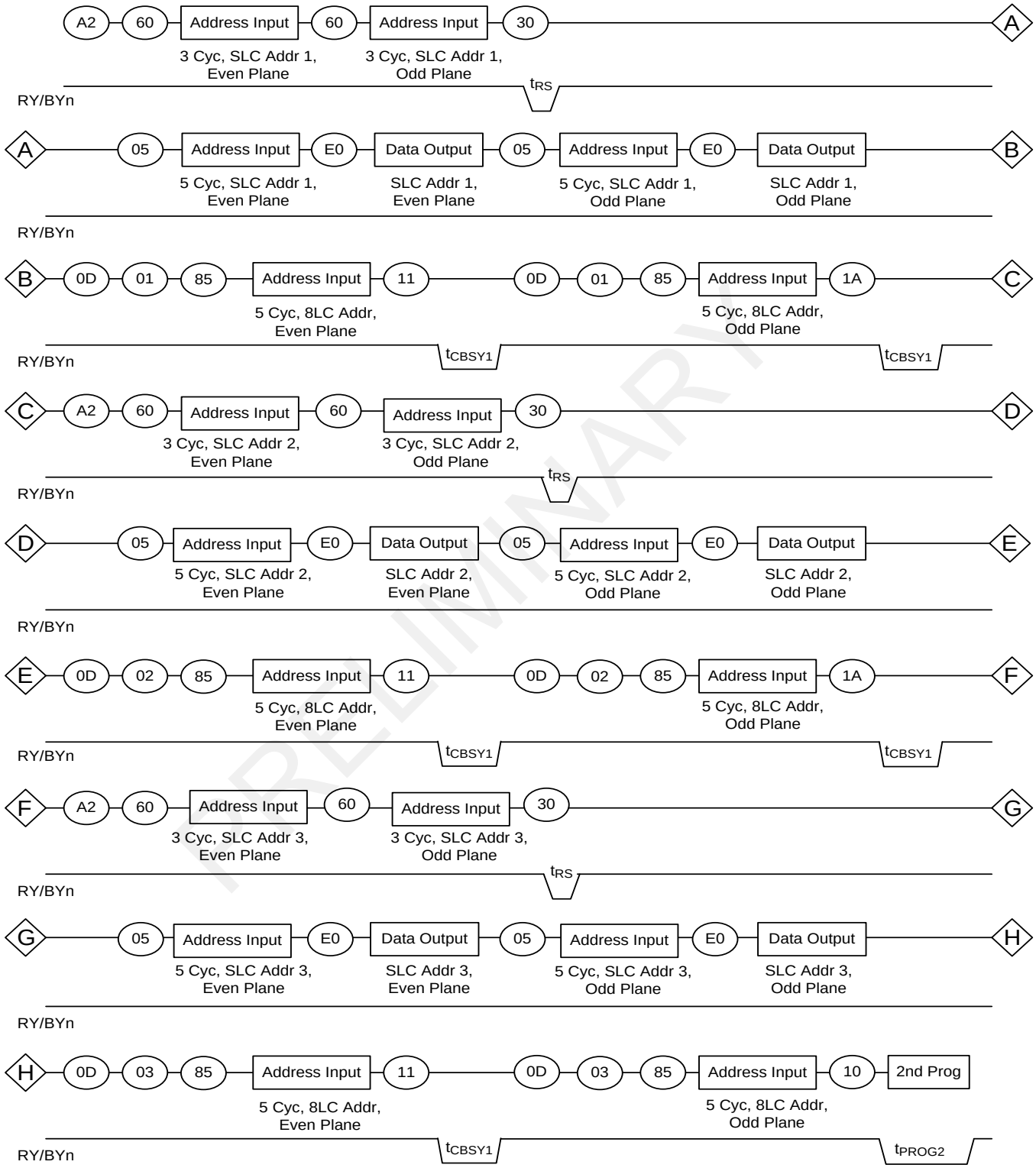
5.13 Multi-Plane Copy Mode (SLC -> 8LC)

The program order defined in section 5.3 must be followed.

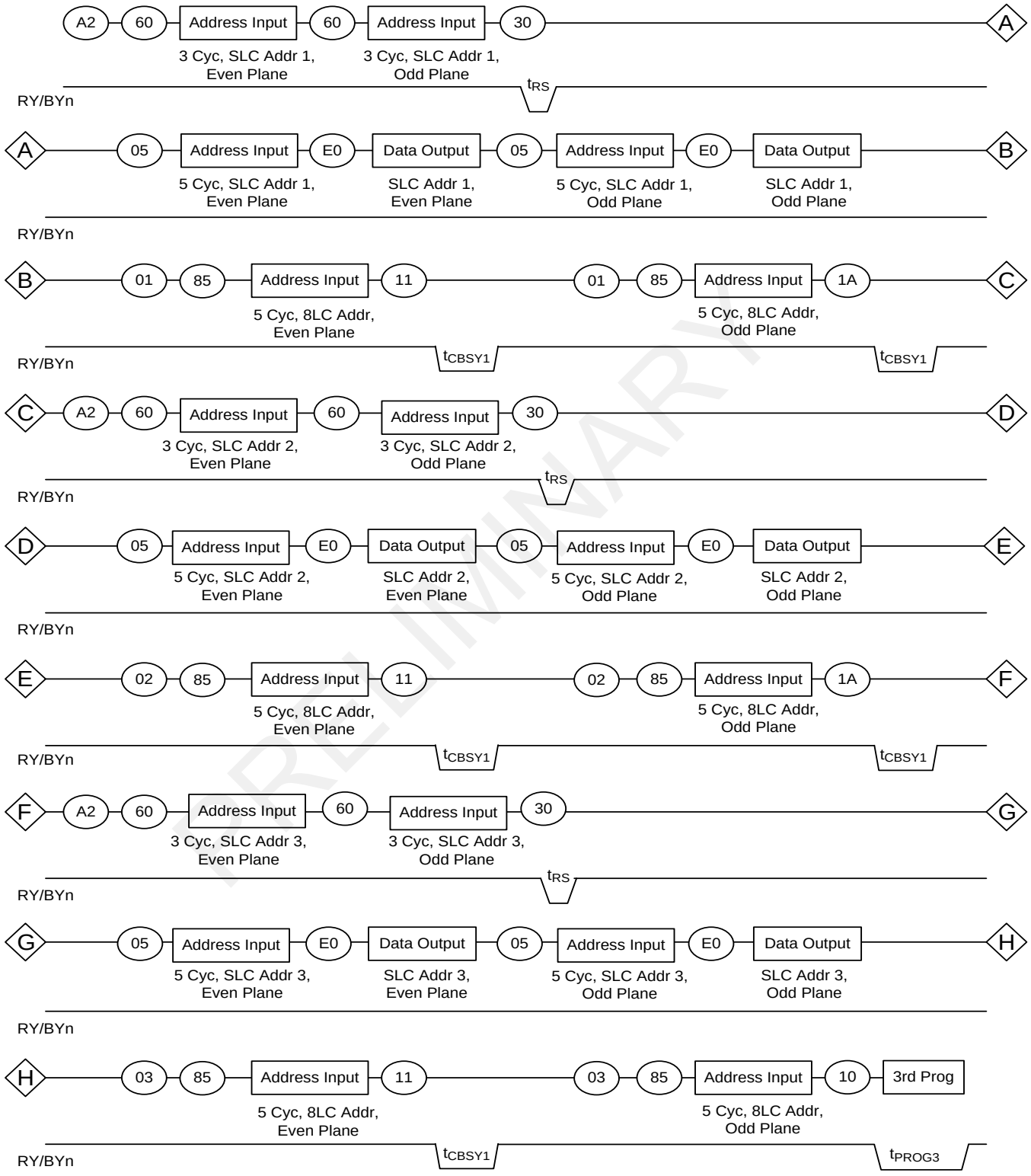
(a) First Copy Cycle



(b) Second Copy Cycle

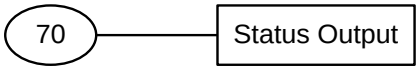


(c) Third Copy Cycle



5.14 Status Read Mode

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using REn after a 70h command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.



Resulting information is outlined in Table 6.

Table 6: 70h Status Read Output

	Definition	Program or Block Erase	Cache Program	Cache Read
I/O0	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O1	Chip Status2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
I/O2	SLC Mode Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O3	SLC Mode Chip Status2 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O4	Not Used	0	0	0
I/O5	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O6	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O0 and I/O1 is valid only during a Normal (8LC) Program/Erase operation when the device is in the Ready state. I/O2 and I/O3 give the device status during the SLC Program/Erase operation.

Chip Status 1:

During a Multi-Plane Program or Multi-Plane Block Erase operation, this bit indicates the pass/fail result.

During a Multi-Plane Program with Data Cache operation, this bit shows the pass/fail results of the current program operation; therefore, this bit is valid only when I/O5 shows the Ready state.

Chip Status 2:

This bit shows the pass/fail result of the previous program operation during Multi-Plane Program with Data Cache. This status is valid when I/O6 shows the Ready state.

The status output on I/O5 is the same as that of I/O6, if the command input just before the 70h is not 15h or 3Ch.

5.15 ID Read Mode

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

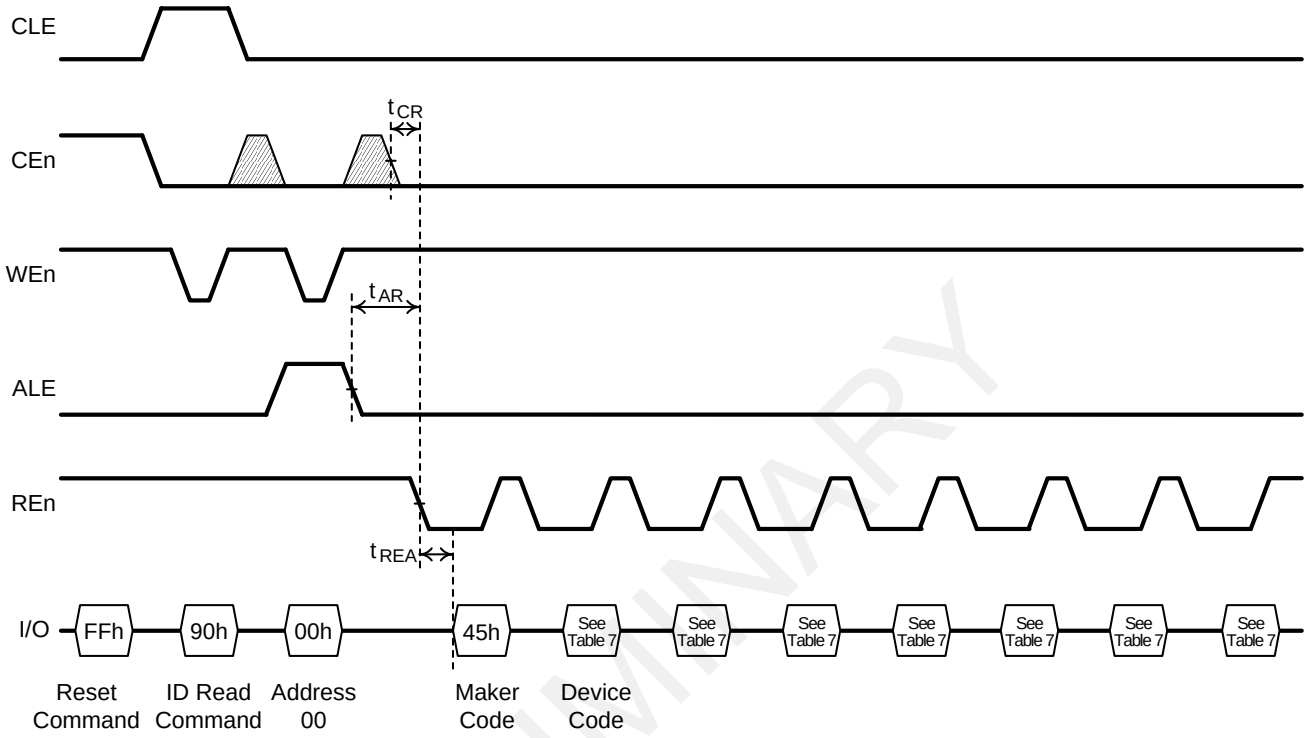


Table 7: ID Code

Address		Items	D7	D6	D5	D4	D3	D2	D1	D0	Hex
00h	**Maker Code**	SanDisk	0	1	0	0	0	1	0	1	45h
01h	**Device Code**	64Gbit (8LC) 3.3V	1	1	0	1	1	1	1	0	DEh
02h	**MLC**	8LC	1	0	0	1	1	0	0	0	98h
03h	**Block Size**	4MB	1	0	0	1	0	0	1	0	92h
04h	**Plane Information**	1 Physical Plane	0	1	1	1	0	0	1	0	72h
05h	**Technology Code**	24nm	0	1	0	1	0	1	1	0	56h
06h	**Reserved**	Reserved	X	X	X	X	X	X	X	X	
07h	**Reserved**	Reserved	X	X	X	X	X	X	X	X	

X = Don't Care

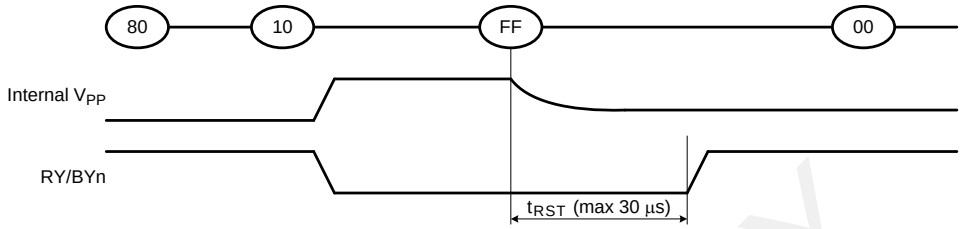
5.16 Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 V and the device enters the Wait state.

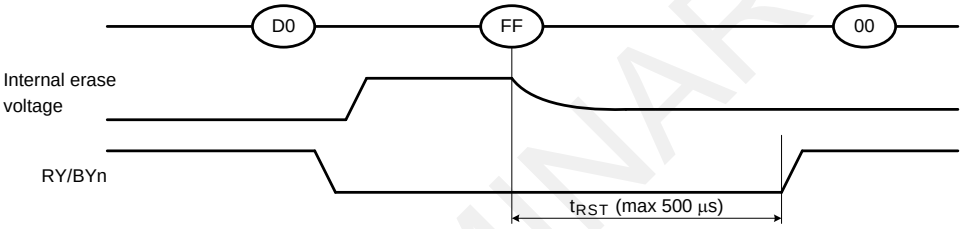
A Reset during a cache program might not stop only the most recent program operation, it might also stop the previous program operation, depending on when the FFh Reset is input.

The response to an FFh Reset command input during the various device operations is as follows:

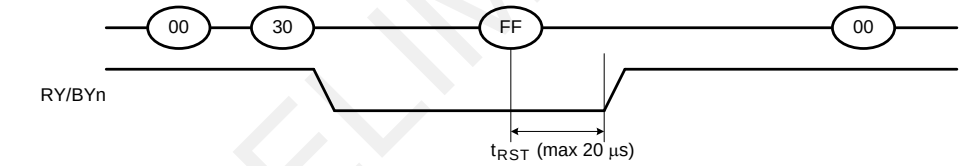
When a Reset (FFh) command is input during programming



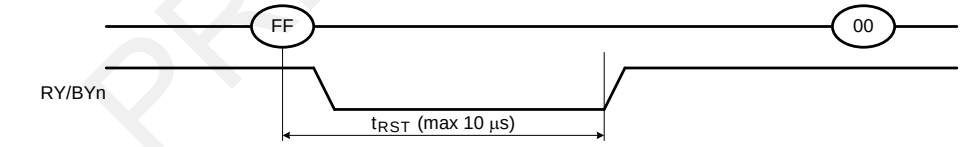
When a Reset (FFh) command is input during erasing



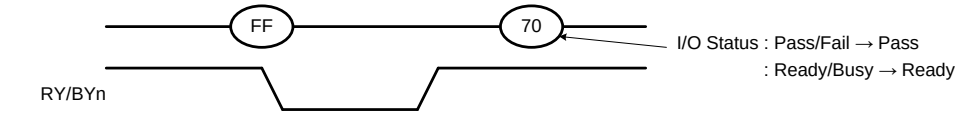
When a Reset (FFh) command is input during a Read operation



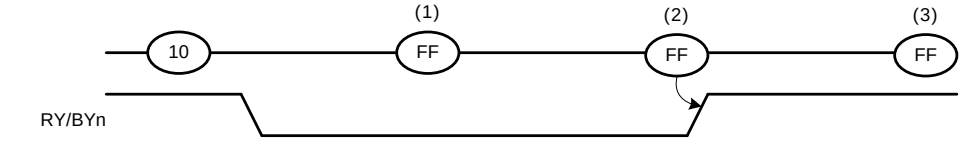
When a Reset (FFh) command is input during Ready



When a Status Read (70h) command is input after a Reset



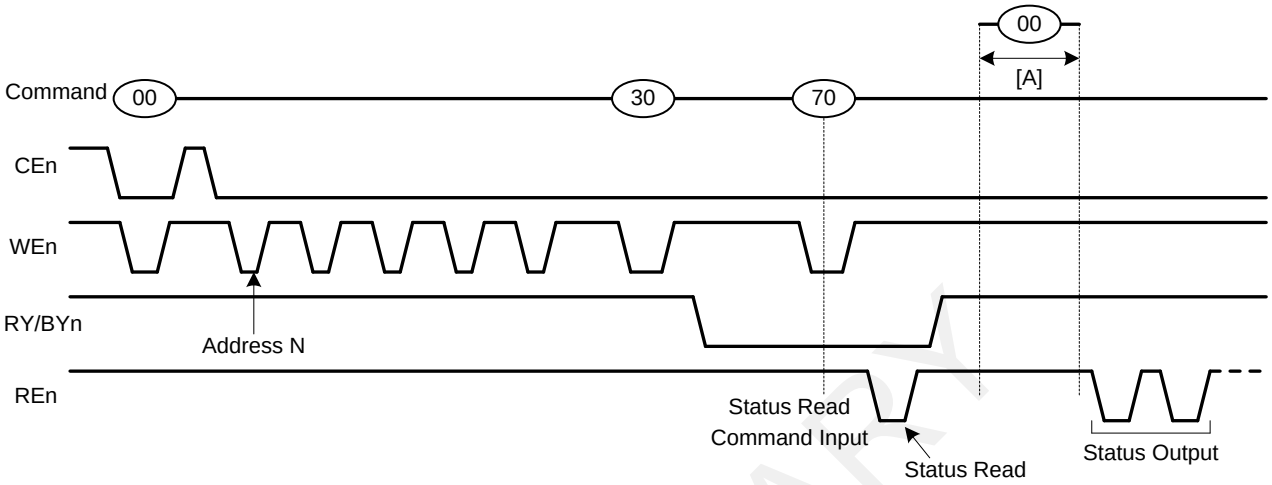
When two or more Reset commands are input in succession



The second FF command is invalid, but the third FF command is valid.

6. Application Notes and Comments

6.1 Status Read During a Read Operation

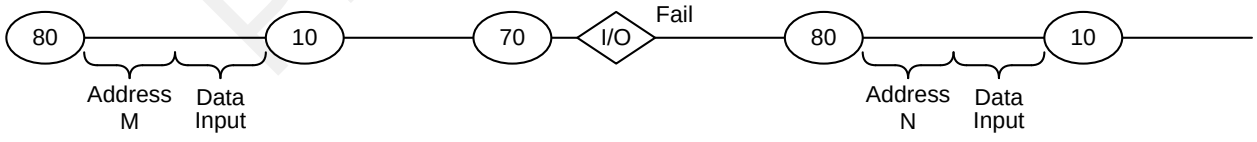


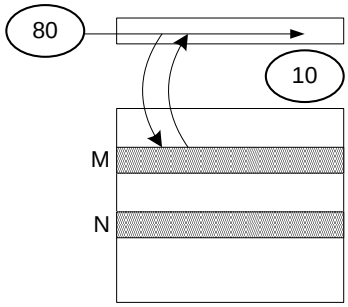
The device status can be read out by inputting the Status Read (70h) command in Read mode. Once the device has been set to Status Read mode by a 70h command, the device does not return to Read mode unless the Read (00h) command is input during [A]. If the Read (00h) command is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

6.2 Erase Before Initial Program Operation

The device might not be erased prior to shipment; therefore, all blocks must be individually erased using the Single-Block Erase command before any Program operation can be performed. The Erase Status can be ignored during this Erase operation. After all of the blocks are erased, the Bad Block Test Flow (described in Section 6.4) can be applied to determine the locations of invalid (bad) blocks on the device.

6.3 Programming Failure

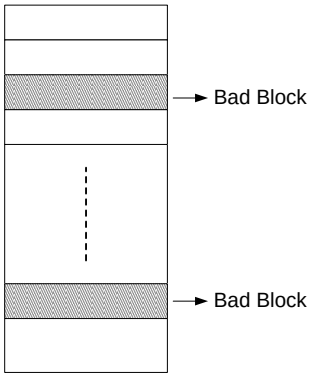




If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.
Because the previous input data has been lost, the same input sequence of 80h command, address, and data is necessary. The proper page address program sequence (defined in Section 5.3) must be observed.

6.4 Invalid Blocks (Bad Blocks)

A device occasionally contains unusable blocks. Therefore, the following issues must be recognized:

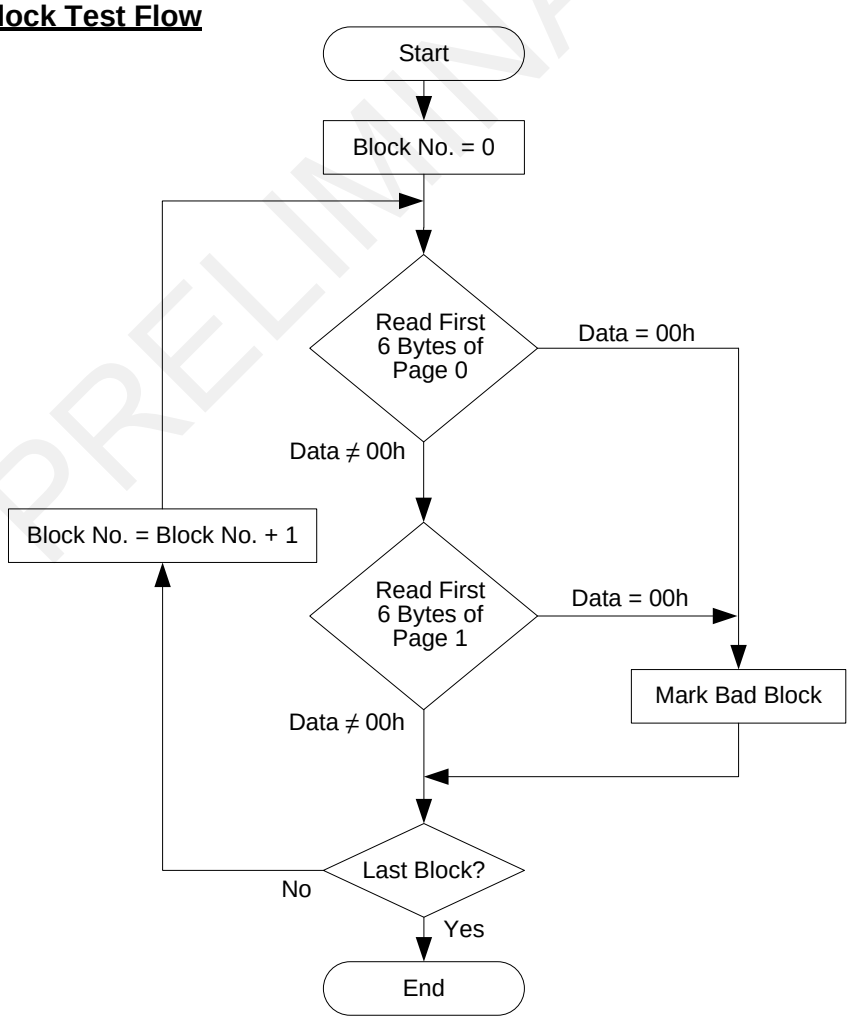


- At the time of shipment, bad block information is marked on each bad block.
- Check the device for any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.
- A small percentage of blocks available on a die might be marked as bad blocks throughout a device's lifetime. The first logical block on each die is guaranteed to be good, and each block identified as good at shipment does not have program/erase status failure upon the first program/erase cycle. A bad block does not affect the performance of good blocks, because it is isolated from the bitlines by select gates.

The number of valid blocks at time of shipment is as follows:

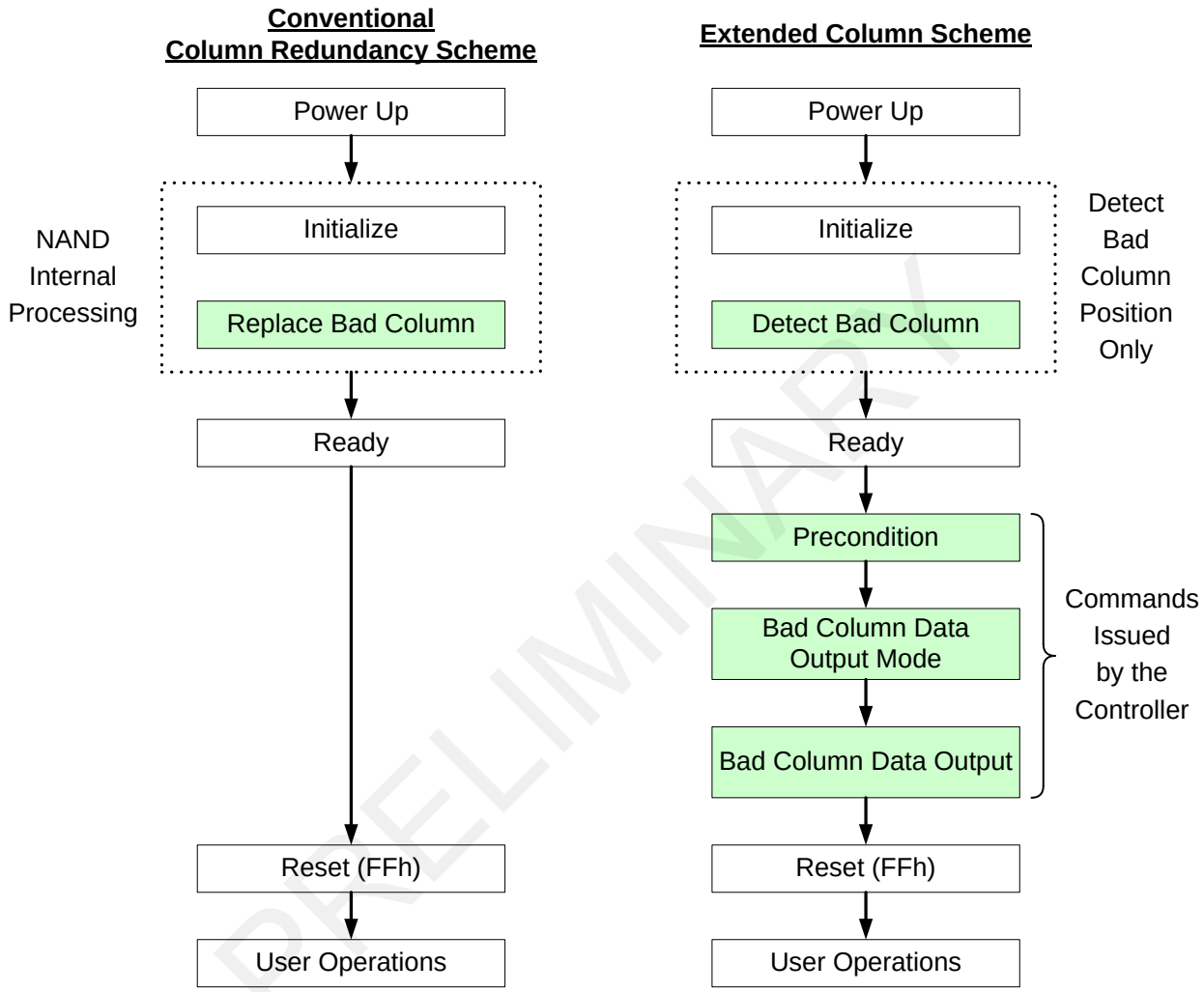
	MIN	TYP	MAX	UNIT
Valid (Good) Block Number	1956	—	2084	Blocks

Bad Block Test Flow



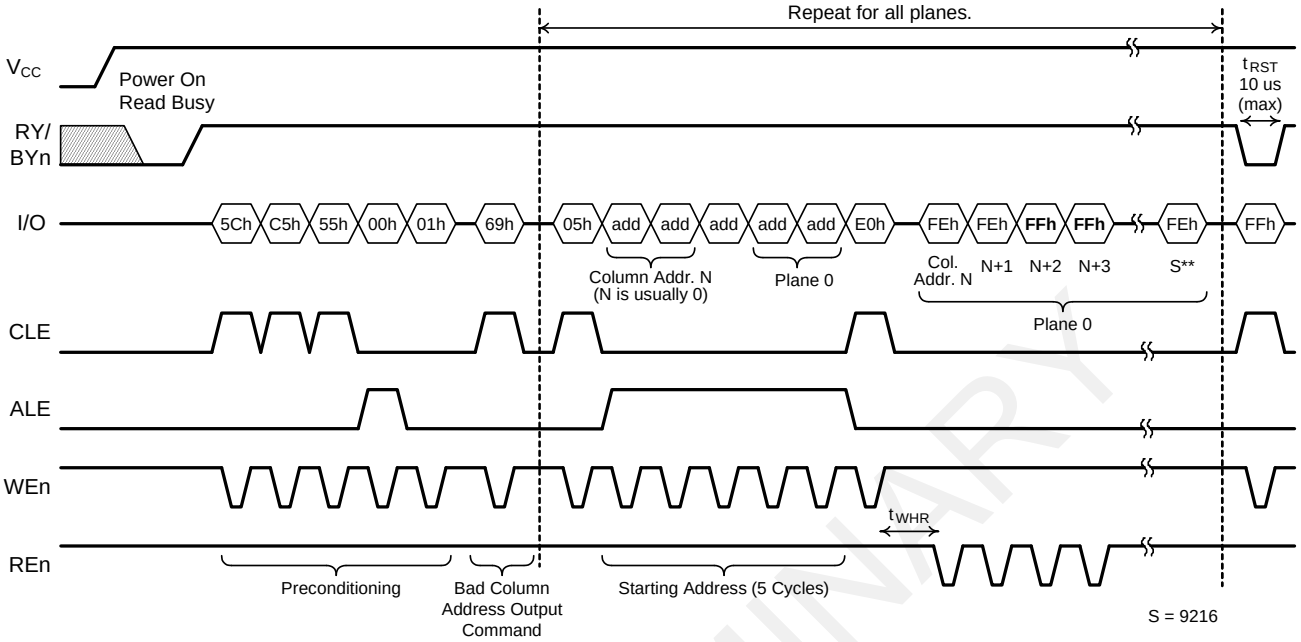
6.5 Bad Column Management

This device uses an extended column scheme to detect and read out bad column information, as shown in the flowchart below:



The bad column address information is stored in the controller which maps each bad column address to a spare column address. There are a total of 1,024 extra bytes available per 8,192 bytes per plane. There can be up to 48 bytes of bad columns per plane at time of shipment. The remaining extra bytes can be used as ECC columns or as spare columns.

Bad Column Data Output Mode Timing



Notes:

(1) Make sure the “Preconditioning Timing Conditions” in section 3.10 are met.

(2) The bad column data is output by REn toggle.
good column -> FEh, bad column -> FFh

(3) Bad columns are reported in a pair of bytes (16 bits). If the $(N+2)^{th}$ byte is bad, then the $(N+3)^{th}$ byte is marked bad (FFh), too.

(4) This mode is terminated with a Reset (FFh) command

(5) The maximum number of bad columns at time of shipment is 48 bytes per plane.

6.6 Dynamic Read Scheme

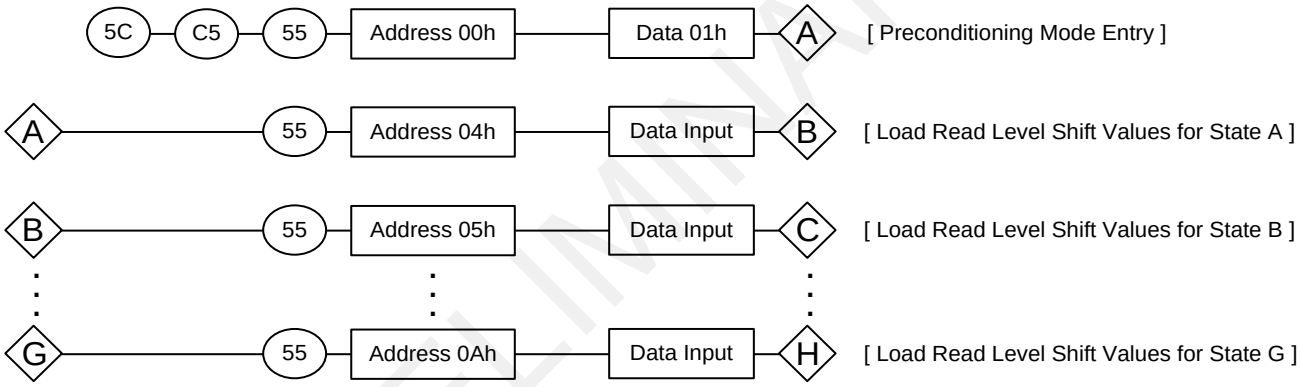
A Dynamic Read Scheme for 8LC Read is provided to allow the Read level for each state to be adjusted to compensate for the shift in threshold voltage distribution, due to charge loss over time. No Dynamic Read is needed for SLC Read.

The normal Read scheme is the default Read mode with a set of initial Read values, and it is used upon every power up. When an uncorrectable error (UECC) is encountered (failure bits exceeding the limit correctable by the ECC algorithm), the Dynamic Read Flag is set to trigger a different set (Case) of Dynamic Read values to be used for all subsequent Reads. Multiple Cases of Dynamic Read values are available to track the threshold voltage shift over time and after cycling. When a UECC is encountered again, the Case Number is incremented.

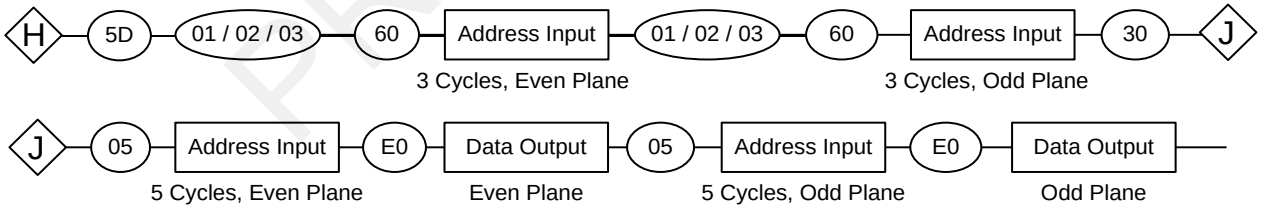
The Dynamic Read Flag, Case Number, and Read Level Shift values are stored by the controller.

Dynamic Read Command Sequence

To Load Dynamic Read Shift Values:



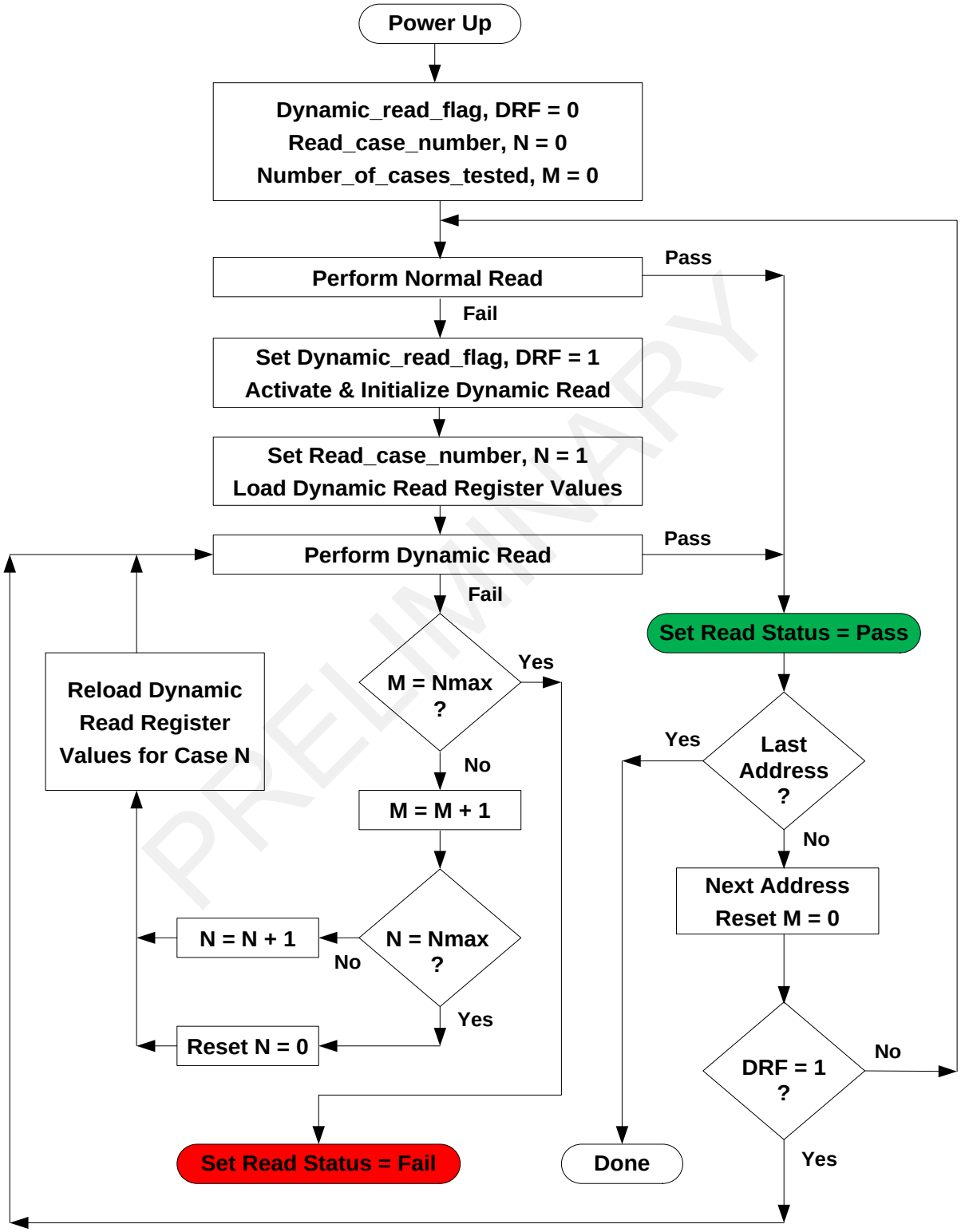
To Perform Dynamic Read:



To Exit:

Dynamic Read Level Shift values for each Case are provided in a separate document.

The Dynamic Read Scheme is illustrated below:



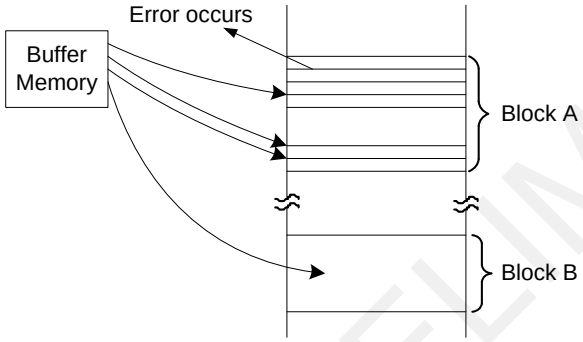
6.7 Failure Phenomena for Program and Erase Operations

The device might fail during a Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.

Failure Mode		Detection And Countermeasure Sequence
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Column	Programming Failure	Status Read after Program → Column Replacement
Random Bit	Programming Failure "1 to 0"	ECC

- ECC: Error Correction Code: TBD
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (by creating a table within the system or by using another appropriate scheme).

6.8 Power Loss

Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before a write/erase operation is complete causes loss of data and/or damage to data.

6.9 Reset Command

If an FFh Reset command is input before completion of a write operation to a page, it might cause damage to data, not only to the programmed page, but also to the adjacent page sharing the same wordline. The proper page address program sequence (defined in Section 5.3) must be observed.

6.10 Reliability Guidance

Although random bit errors might occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes might be recovered by a block erase. ECC treatment for read data is mandatory, due to the following Data Retention and Read Disturb failures.

- **Write/Erase Endurance**

  Write/Erase endurance failures might occur in a cell, page, or block, and are detected by doing a status read after either a program or a block erase operation. The cumulative bad block count increases along with the number of write/erase cycles.

- **Data Retention**

  The data in memory might change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block might become usable again.

- **Read Disturb**

  A read operation might disturb the data in memory. The data might change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge might build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block might become usable again.

All reliability-related parameters and results are measured using a random data pattern stored in memory. Results might differ if other data patterns are used.