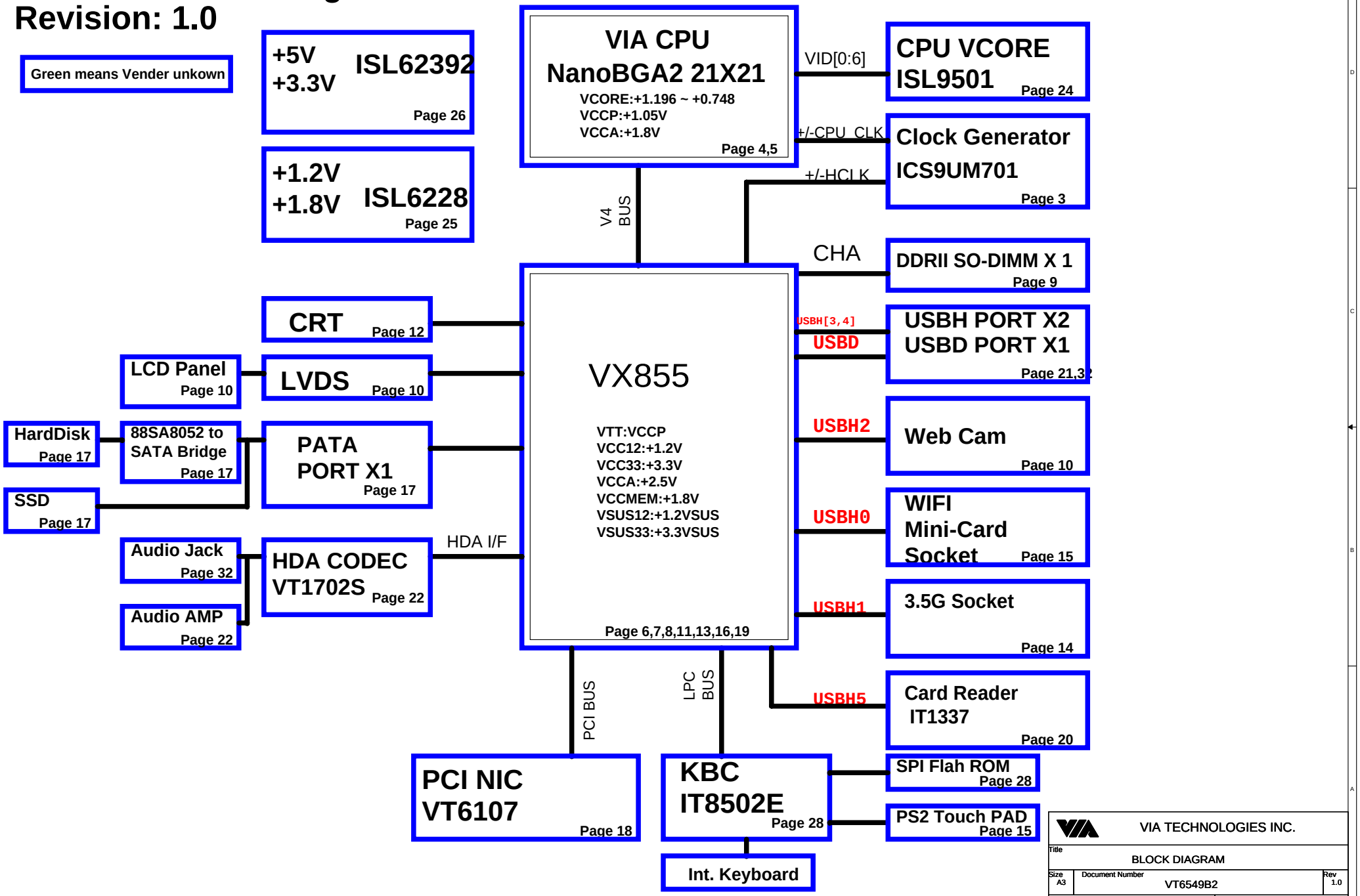
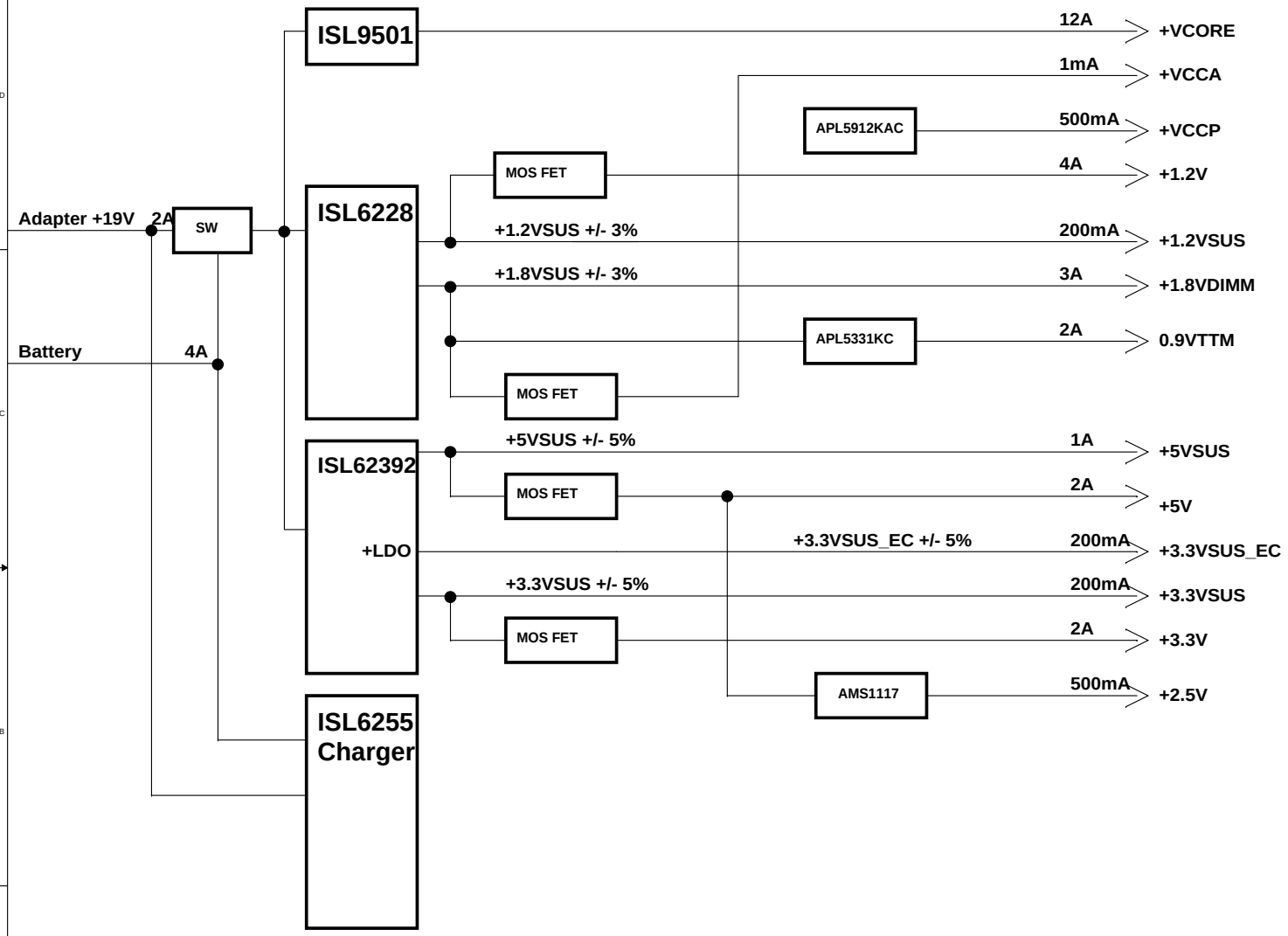
VT6549B2 Block Diagram
Revision: 1.0



VIA TECHNOLOGIES INC.		
Title: BLOCK DIAGRAM		
Size: A3	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 1 of 35	



S0/S1	S3	S4	S5	DEVICE	TEST PAD
X				CPU	TP26
X				CPU (1.8V)	TP32
X				CPU (1.05V)	TP31
X				VX855 core	TP30
X	X	X		VX855 SUS1.2V	TP28
X	X			DDR VX855 DDR	TP33
X				DDR VTTM	TP34
X				USB	TP46
X				AUDIO CODEC	TP47
X	X	X	X	EC	
X	X			VX855 SUS3.3V	TP27
X				VX855 ,I/O	TP29
X				VX855 2.5V	TP35

VIA TECHNOLOGIES INC.

Title: POWER BLACK DIAGRAM

Size: A3 | Document Number: VT6549B2 | Rev: 1.0

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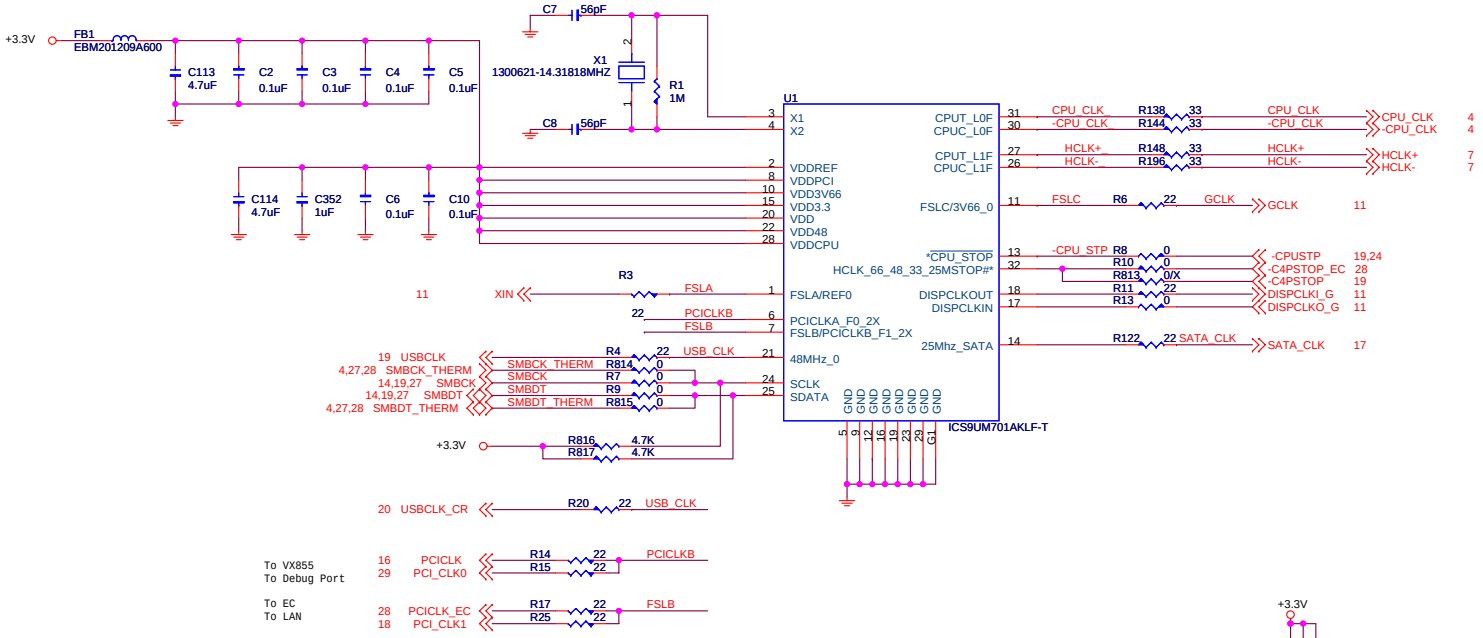

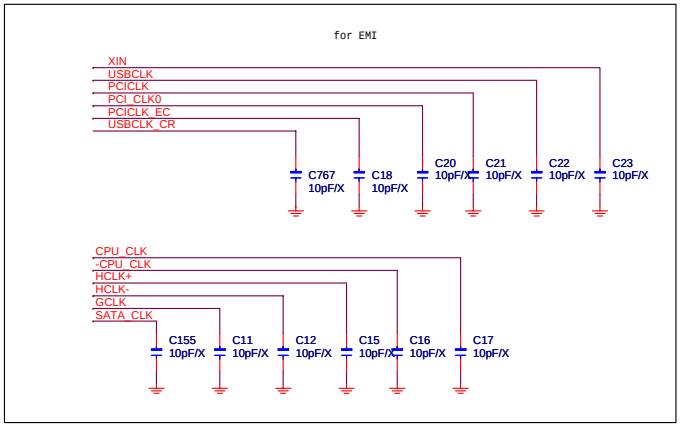

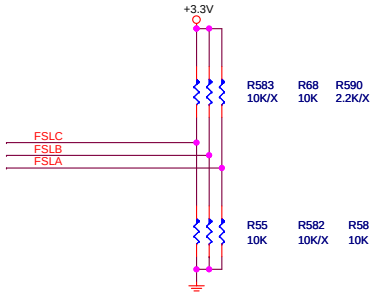

CLOCK Strapping

R590	R583	R68	1	
R58	R55	R582	0	
FSLA	FSLC	FSLB	CPU	PCI
1	0	0	133.33	33
0	0	1	200	33
1	1	0	100	33

VIA TECHNOLOGIES INC.

Title: CLK GEN - ICS9UM702/703

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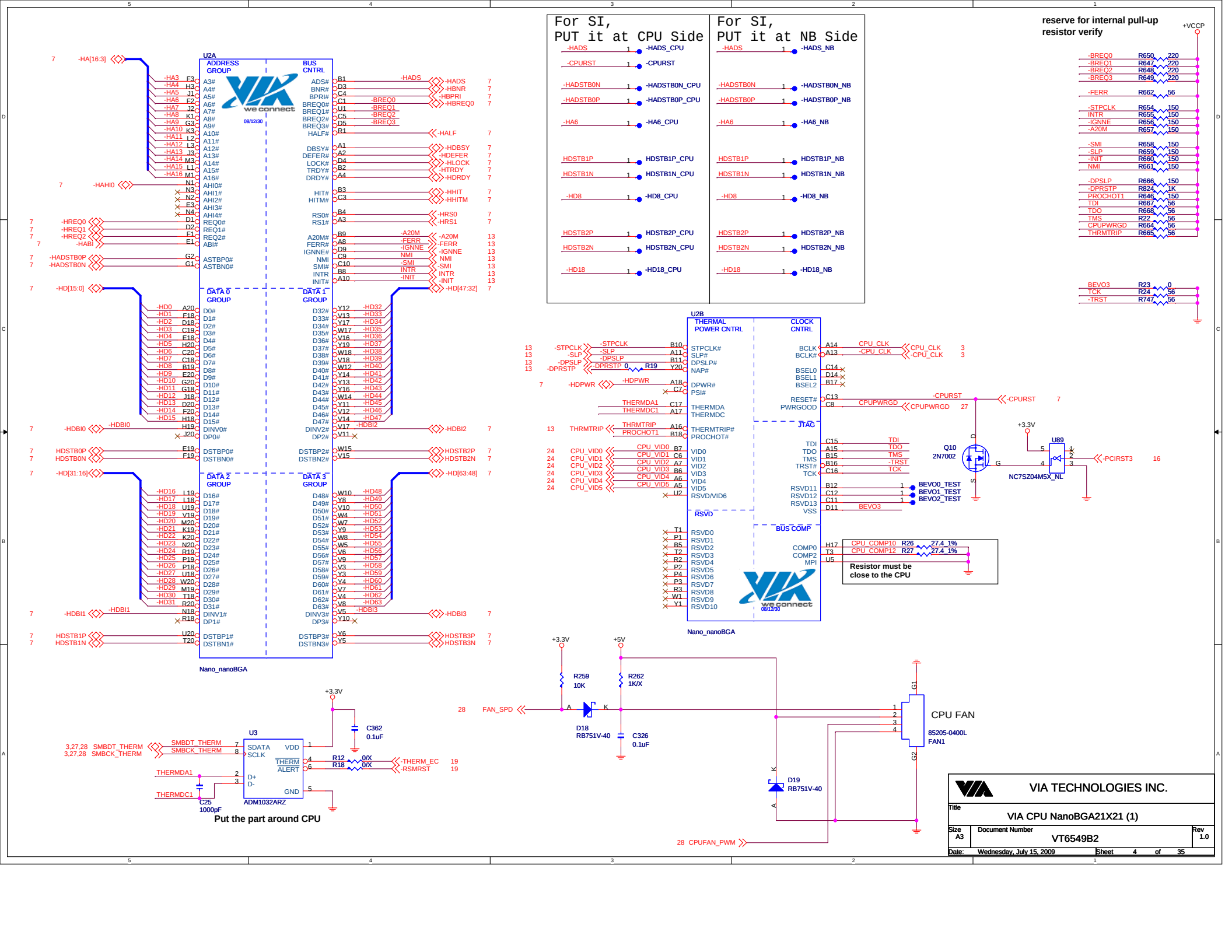
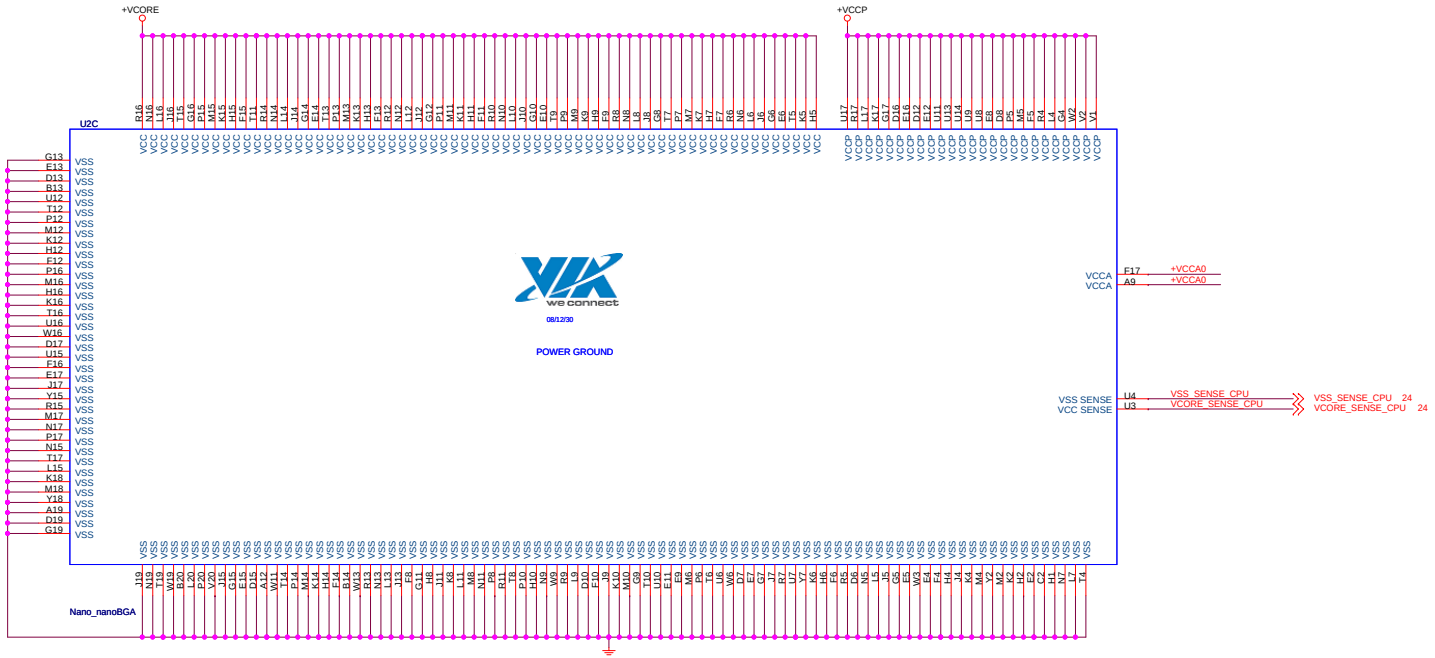
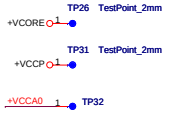

For SI, PUT it at CPU Side
For SI, PUT it at NB Side
reserve for internal pull-up resistor verify
U2A
ADDRESS GROUP
BUS CNTRL
DATA 0 GROUP
DATA 1 GROUP
DATA 2 GROUP
DATA 3 GROUP
Nano_nanoBGA
U2B
THERMAL POWER CNTRL
CLOCK CNTRL
JTAG
RSVD
BUS COMP
Nano_nanoBGA
Resistor must be close to the CPU
U3
ADM1032ARZ
Put the part around CPU
CPU FAN
85205-0400L
FAN1
VIA TECHNOLOGIES INC.
VIA CPU NanoBGA21X21 (1)
VT6549B2
Wednesday, July 15, 2009

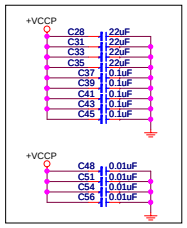




Put the caps. on the bottom of CPU.
Please refer to the placement below.

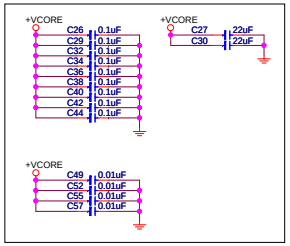
VCCP: 22uF x 4
0.1uF x 5
0.01uF x 4

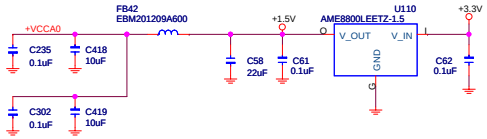
+VCCP Capacitor under CPU



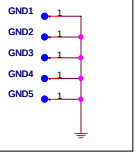
VCORE: 22uF x 2
0.1uF x 9
0.01uF x 4

+VCORE Capacitor under CPU

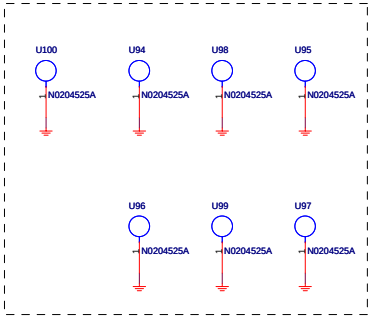




Put the test point on Top side and be close to the CPU

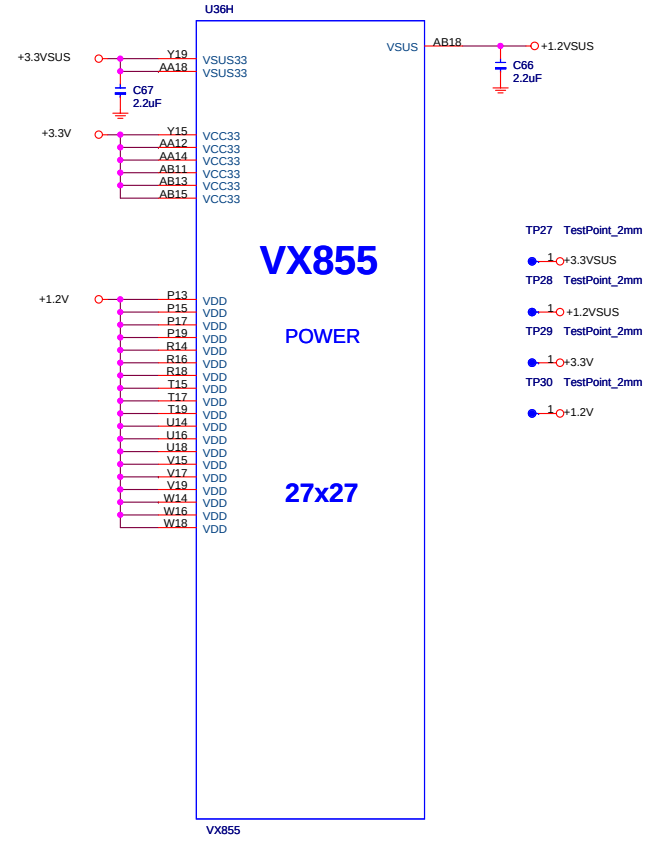


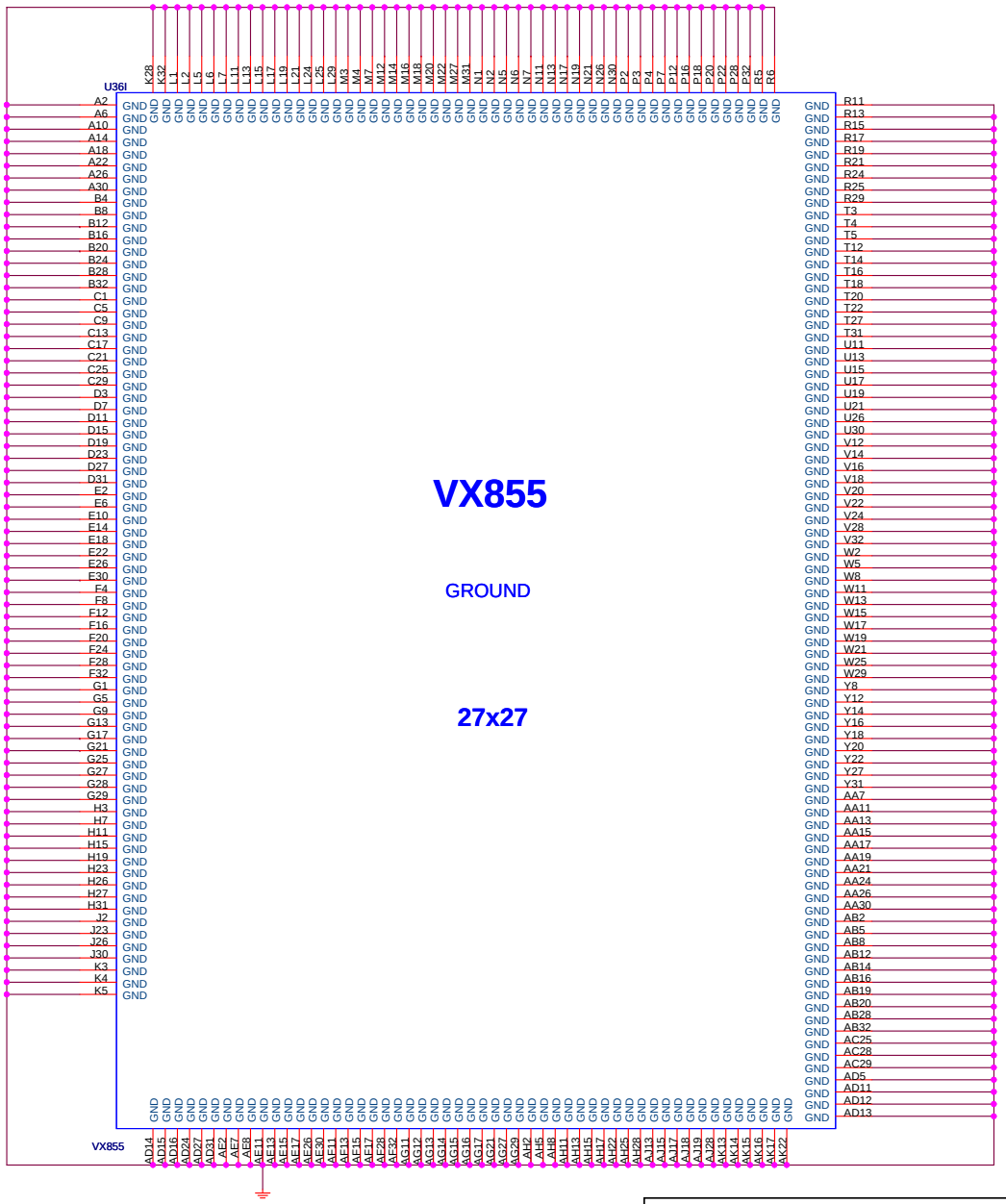
CPU HEAT SINK



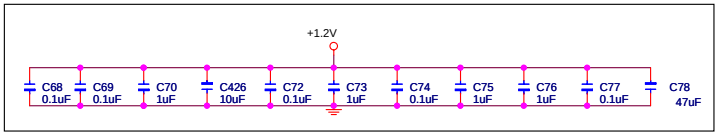
NUT COPPER N0204525A
Circle,M2.5*4.5*3.6mm
Part number:99G45-010034

VIA TECHNOLOGIES INC.		
Title: VIA CPU NanoBGA21X21 (2)		
Size: C	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 5 of 35	

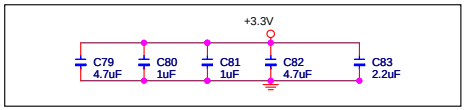




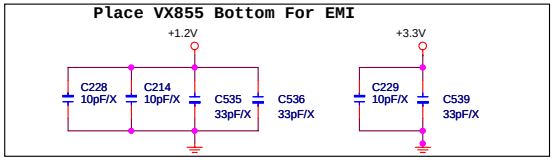
Place VX855 Bottom



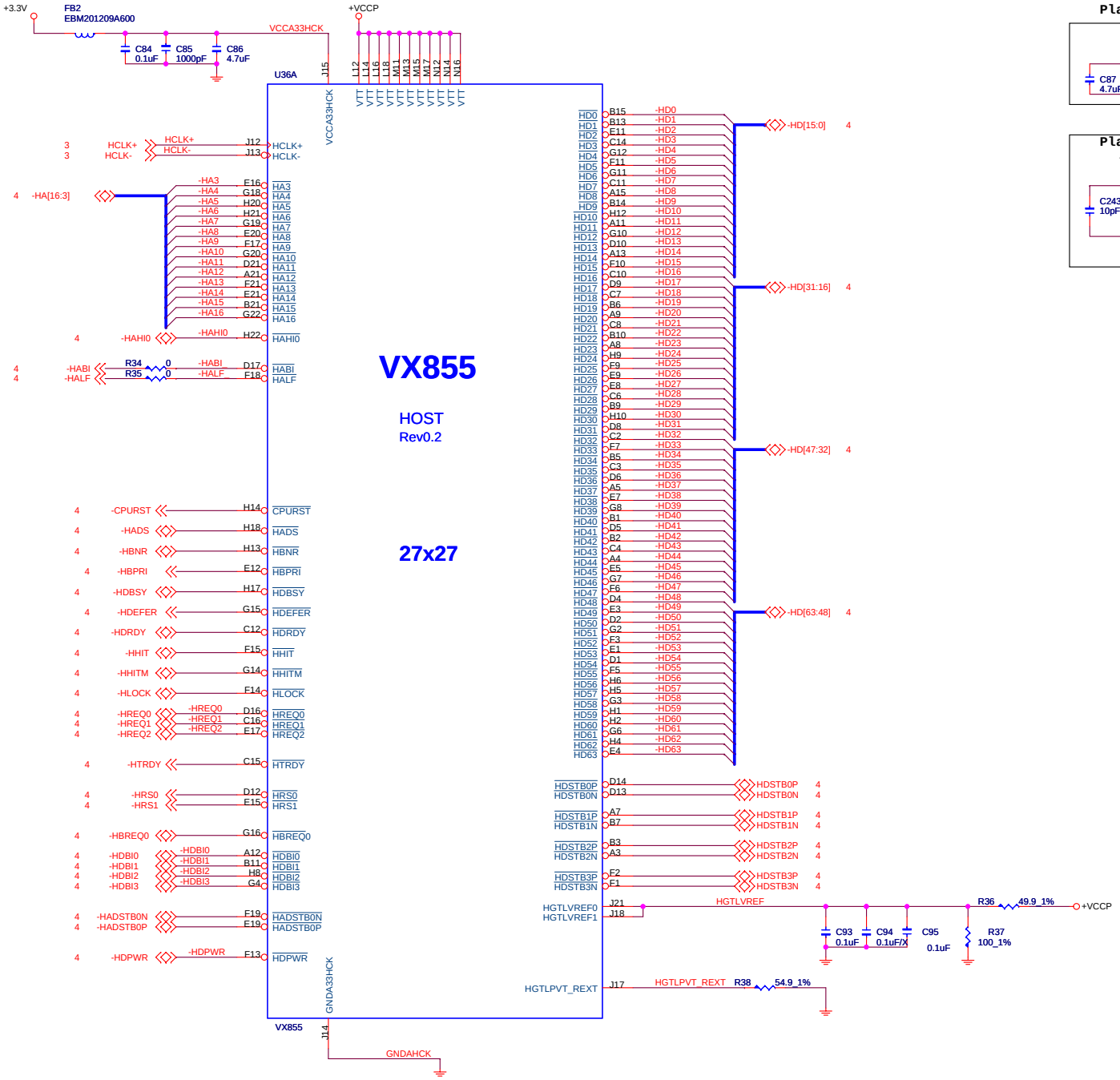
Place VX855 Bottom



Place VX855 Bottom For EMI

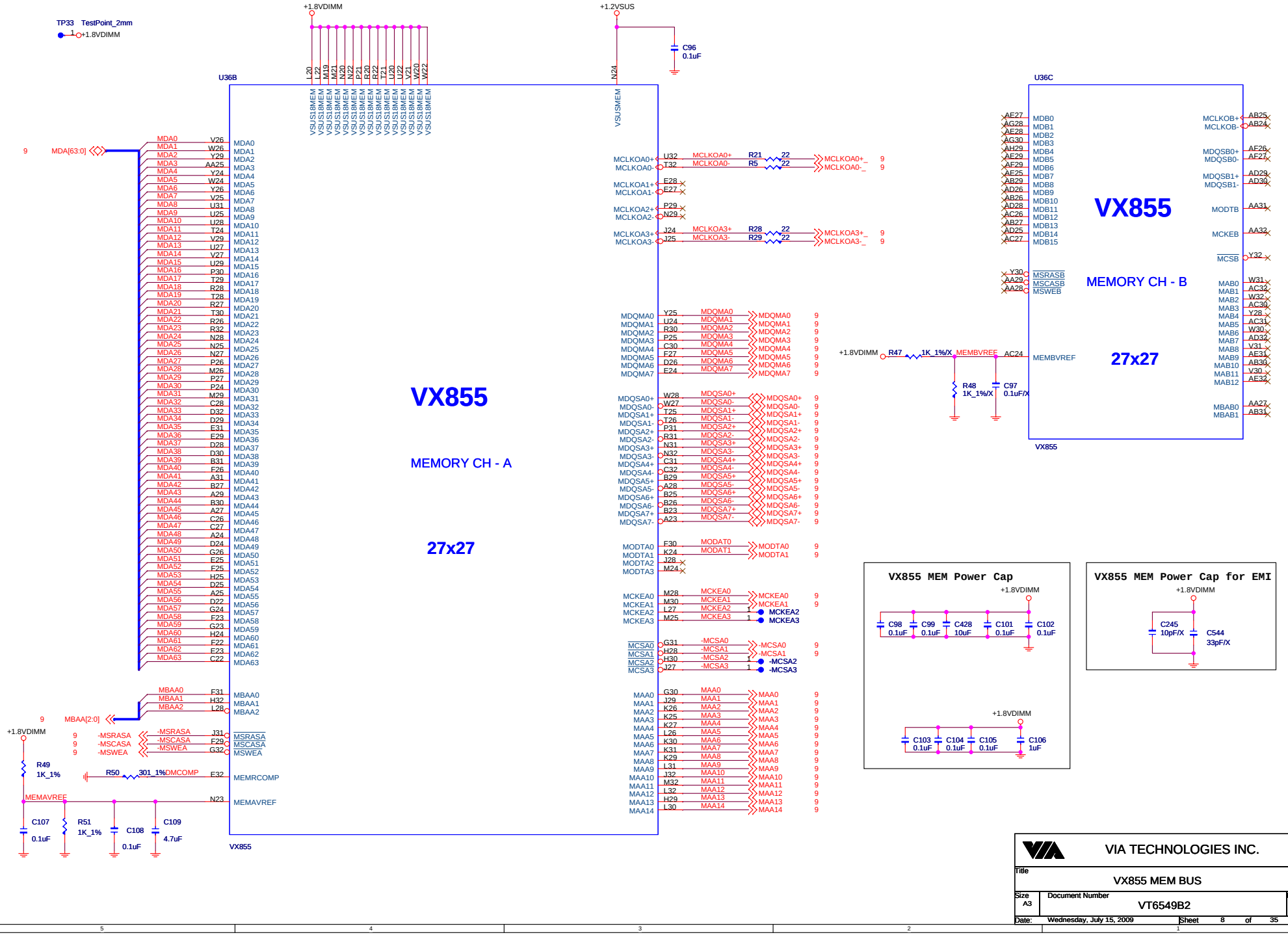


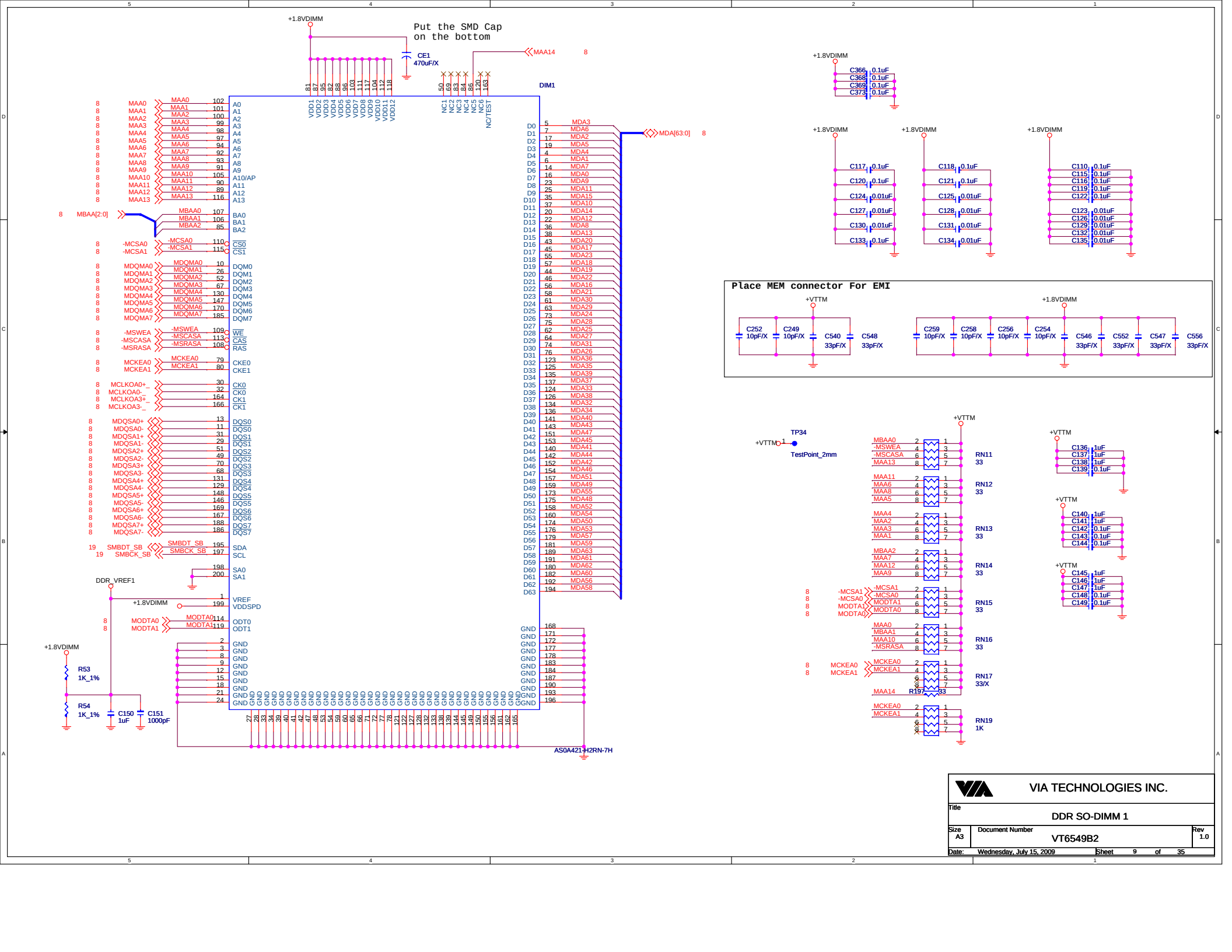
VIA TECHNOLOGIES INC.		
Title: VX855 Power&Ground		
Size: A3	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 6 of 35	



VIA TECHNOLOGIES INC.

Title	VX855 HOST BUS	
Size A3	Document Number VT6549B2	Rev 1.0
Date: Wednesday, July 15, 2009	Sheet 7 of 35	


TP33 TestPoint_2mm
+1.8VDIMM
+1.2VSUS
C96 0.1uF
U36B
VX855
MEMORY CH - A
27x27
MDA[63:0]
MBAA[2:0]
-MSRASA
-MSCASA
-MSWEA
MEMRCOMP
MEMAVREF
R49 1K_1%
R50 301_1%
DMCOMP
C107 0.1uF
R51 1K_1%
C108 0.1uF
C109 4.7uF
MCLKOA0+
MCLKOA0-
MCLKOA1+
MCLKOA1-
MCLKOA2+
MCLKOA2-
MCLKOA3+
MCLKOA3-
MDQMA0
MDQMA1
MDQMA2
MDQMA3
MDQMA4
MDQMA5
MDQMA6
MDQMA7
MDQSA0+
MDQSA0-
MDQSA1+
MDQSA1-
MDQSA2+
MDQSA2-
MDQSA3+
MDQSA3-
MDQSA4+
MDQSA4-
MDQSA5+
MDQSA5-
MDQSA6+
MDQSA6-
MDQSA7+
MDQSA7-
MODTA0
MODTA1
MCKEA0
MCKEA1
MCKEA2
MCKEA3
-MCSA0
-MCSA1
-MCSA2
-MCSA3
MAA0
MAA1
MAA2
MAA3
MAA4
MAA5
MAA6
MAA7
MAA8
MAA9
MAA10
MAA11
MAA12
MAA13
MAA14
U36C
VX855
MEMORY CH - B
27x27
MDB0
MDB1
MDB2
MDB3
MDB4
MDB5
MDB6
MDB7
MDB8
MDB9
MDB10
MDB11
MDB12
MDB13
MDB14
MDB15
MSRASB
MSCASB
MSWEB
MEMBVREF
R47 1K_1%/X
R48 1K_1%/X
C97 0.1uF/X
MCLKOB+
MCLKOB-
MDQSB0+
MDQSB0-
MDQSB1+
MDQSB1-
MODTB
MCKEB
MCSB
MAB0
MAB1
MAB2
MAB3
MAB4
MAB5
MAB6
MAB7
MAB8
MAB9
MAB10
MAB11
MAB12
MBAB0
MBAB1
VX855 MEM Power Cap
C98 0.1uF
C99 0.1uF
C428 10uF
C101 0.1uF
C102 0.1uF
C103 0.1uF
C104 0.1uF
C105 0.1uF
C106 1uF
VX855 MEM Power Cap for EMI
C245 10pF/X
C544 33pF/X
VIA TECHNOLOGIES INC.
Title
VX855 MEM BUS
Size A3
Document Number VT6549B2
Rev 1.0
Date: Wednesday, July 15, 2009
Sheet 8 of 35


Put the SMD Cap
on the bottom
+1.8VDIMM
CE1
470uF/X
DIM1
MAA14
MDA[63:0]
MBAA[2:0]
DDR_VREF1
+1.8VDIMM
R53
1K_1%
R54
1K_1%
C150
1uF
C151
1000pF
AS0A421-H2RN-7H
Place MEM connector For EMI
+VTTM
C252
10pF/X
C249
10pF/X
C540
33pF/X
C548
33pF/X
C259
10pF/X
C258
10pF/X
C256
10pF/X
C254
10pF/X
C546
33pF/X
C552
33pF/X
C547
33pF/X
C556
33pF/X
TP34
TestPoint_2mm
RN11
RN12
RN13
RN14
RN15
RN16
RN17
RN19
33
33/X
1K
R197
VIA TECHNOLOGIES INC.
Title
DDR SO-DIMM 1
Size
A3
Document Number
VT6549B2
Rev
1.0
Date:
Wednesday, July 15, 2009
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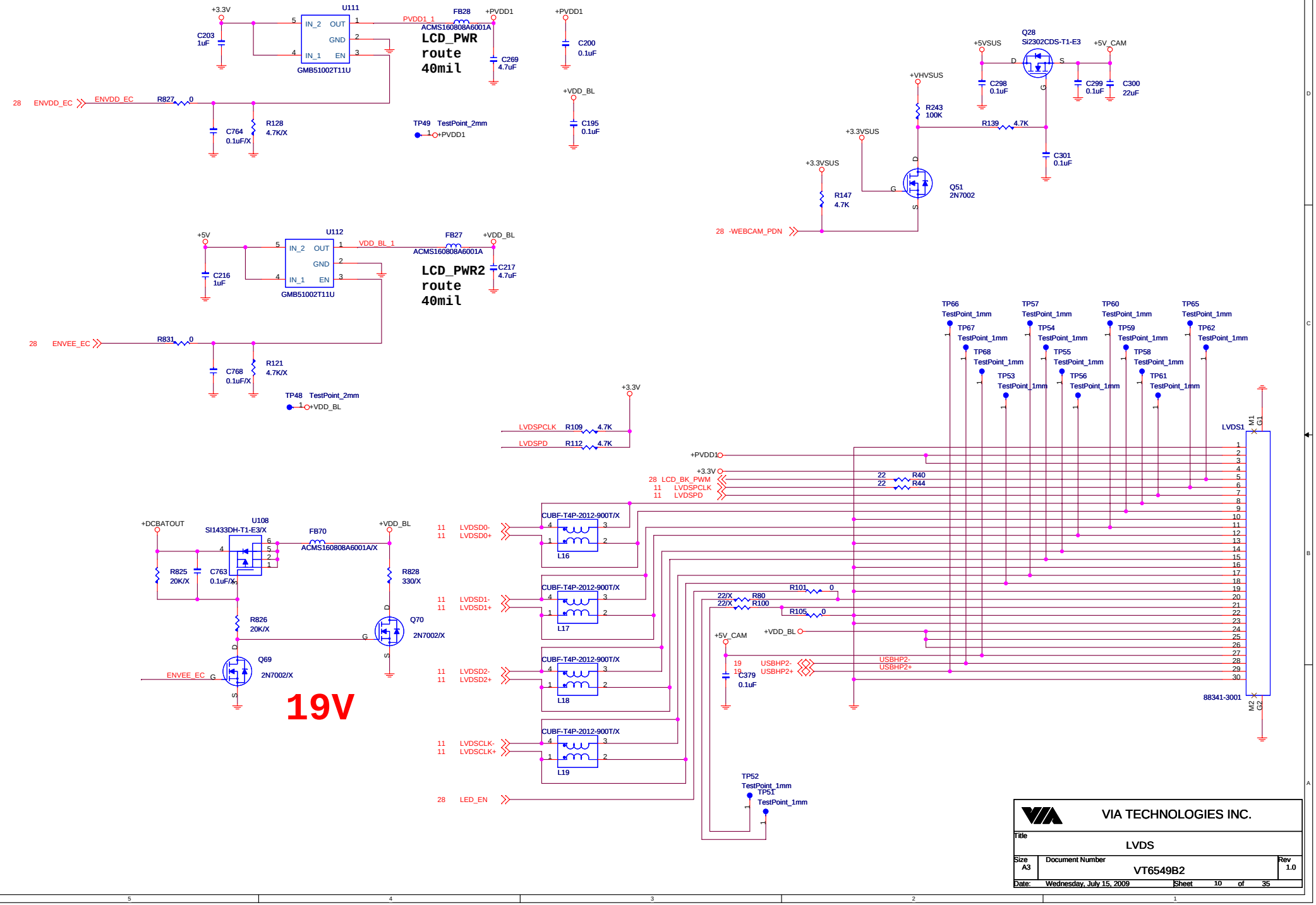
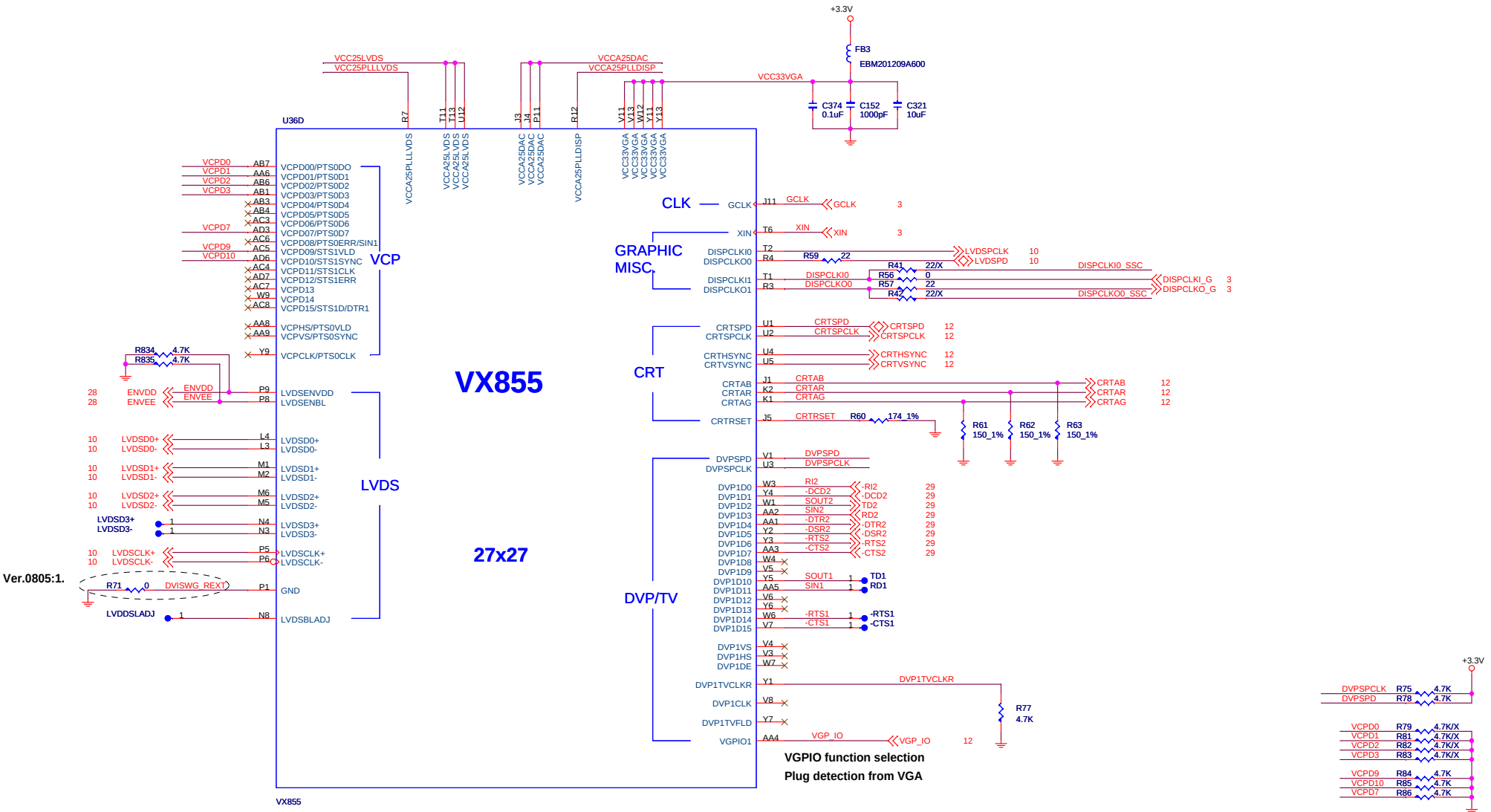
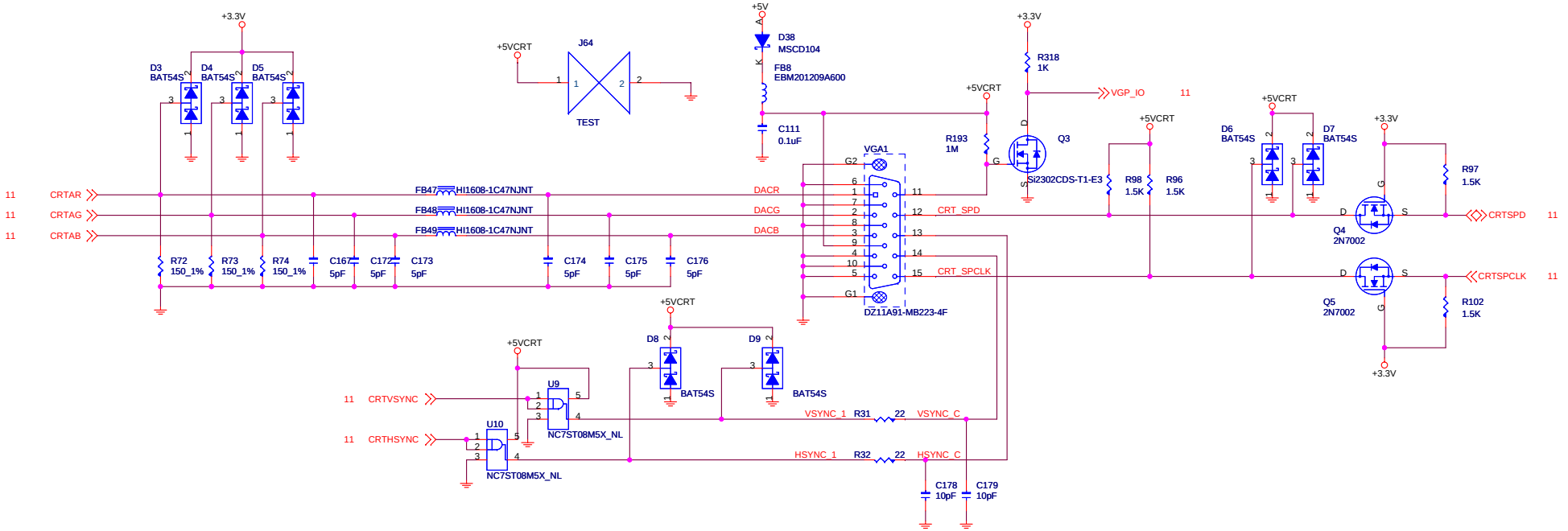
PANEL POWER AND BACKLIGHT CONTROL



VIA TECHNOLOGIES INC.		
Title: LVDS		
Size: A3	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 10 of 35	



VIA TECHNOLOGIES INC.		
Title: VX855-VIDEO BUS		
Size: A3	Document Number: VT6549B2	Rev: 1.0
Date: Monday, July 20, 2009	Sheet 11 of 35	



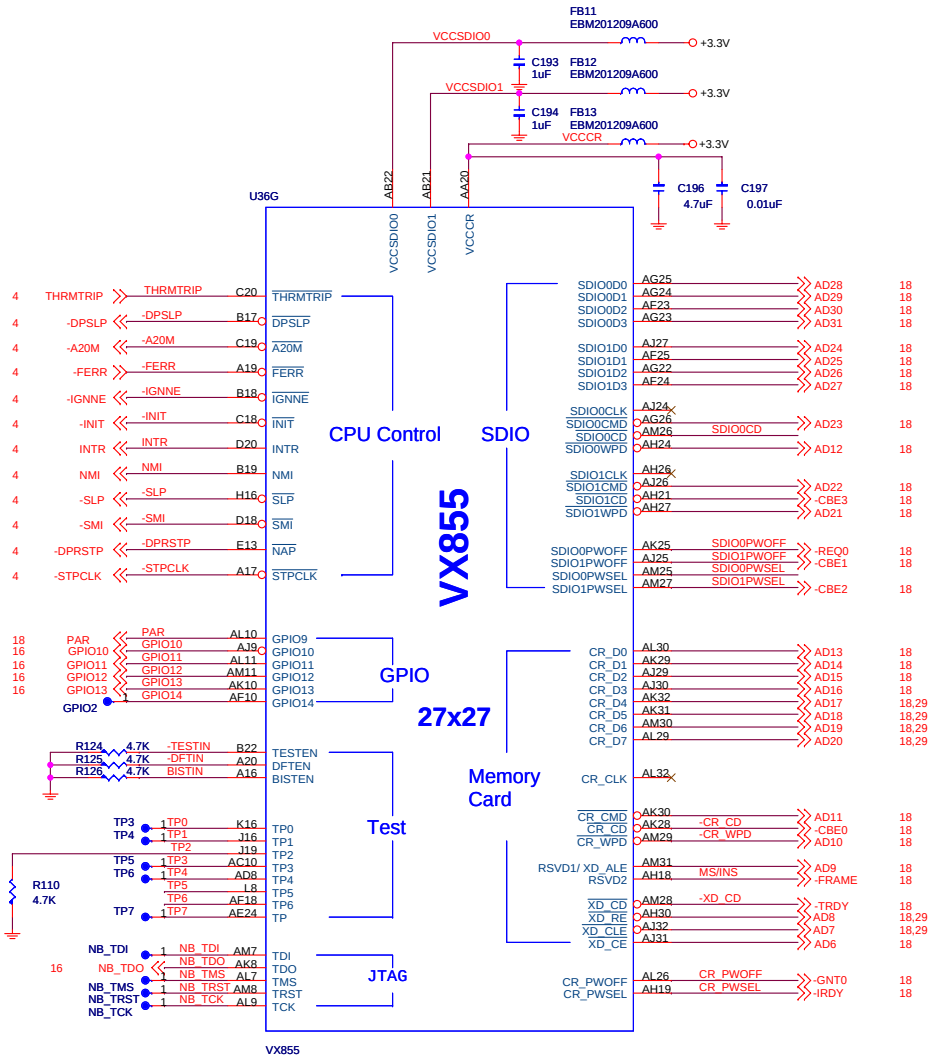
NEAR CONNECTOR

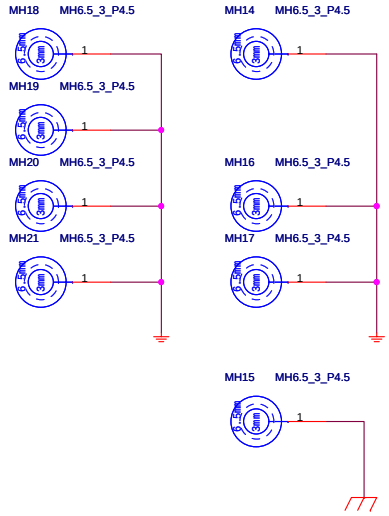
+PVDD1 +PVDD1 +PVDD1 +VDD_BL +VDD_BL

C186 0.1uF C187 4.7uF C188 0.1uF C189 0.1uF C190 4.7uF

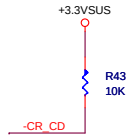
VIA TECHNOLOGIES INC.

Title	CRT	
Size A3	Document Number VT6549B2	Rev 1.0
Date: Wednesday, July 15, 2009	Sheet 12 of 35	

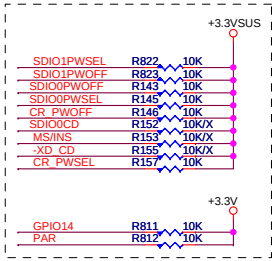




Ver.0708 6.

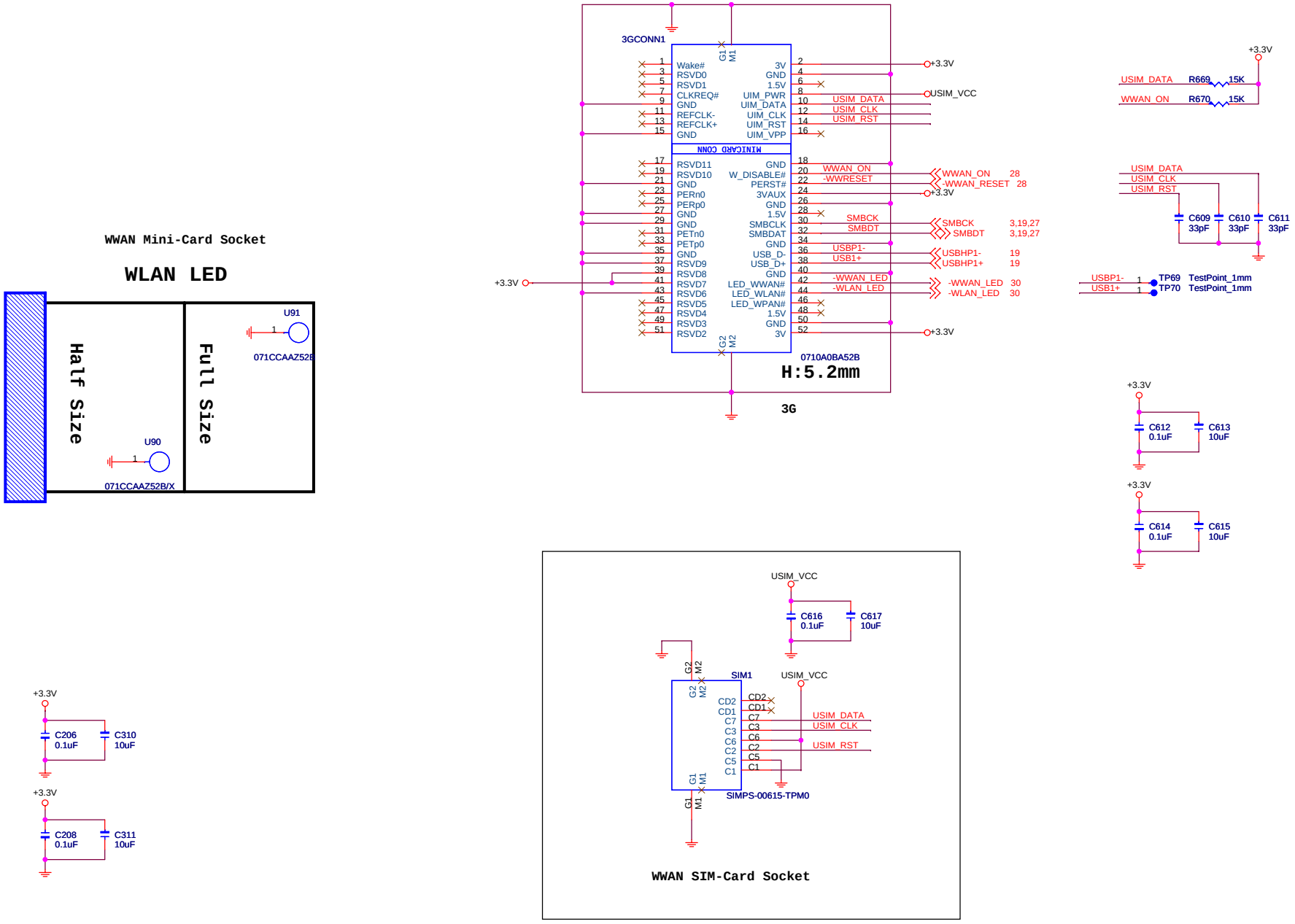


reserve for internal pull-up resistor verify



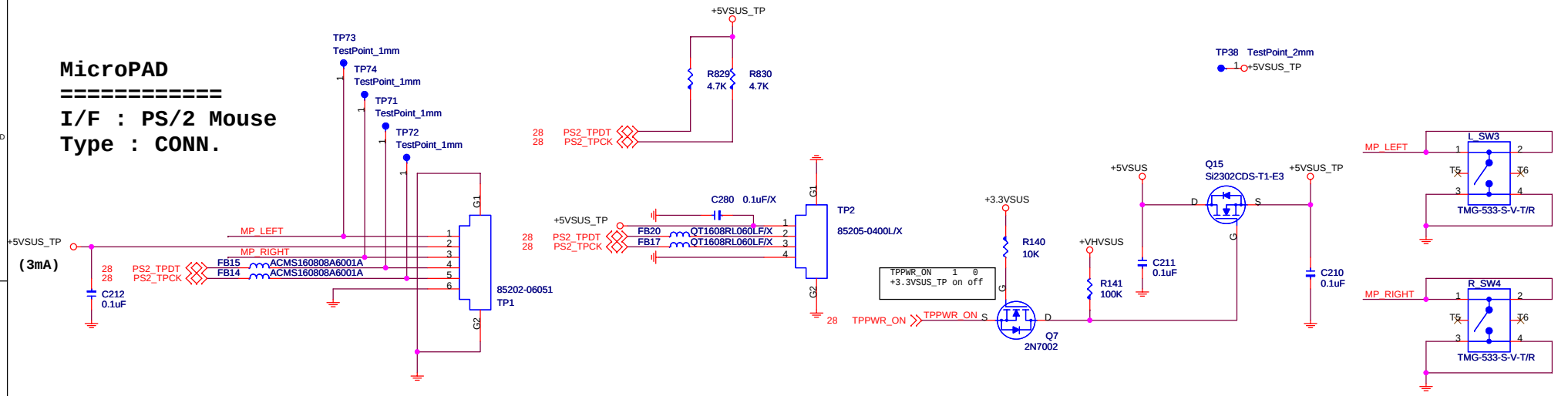
VIA TECHNOLOGIES INC.

Title	VX855 PCI	
Size A3	Document Number VT6549B2	Rev 1.0
Date: Wednesday, July 15, 2009	Sheet 13 of 35	



VIA TECHNOLOGIES INC.		
Title: Mini-Card &SIM		
Size	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 14 of 35	

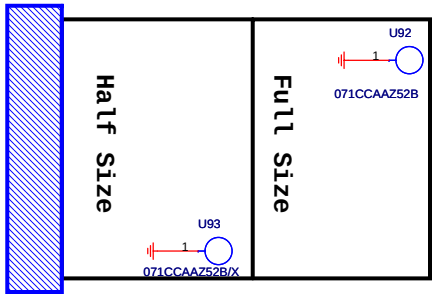
MicroPAD
==========
I/F : PS/2 Mouse
Type : CONN.



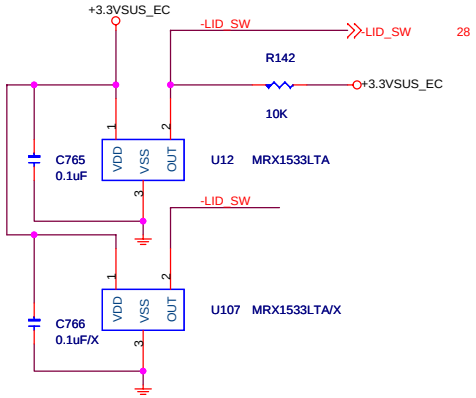
Synaptics TM61PUAG214

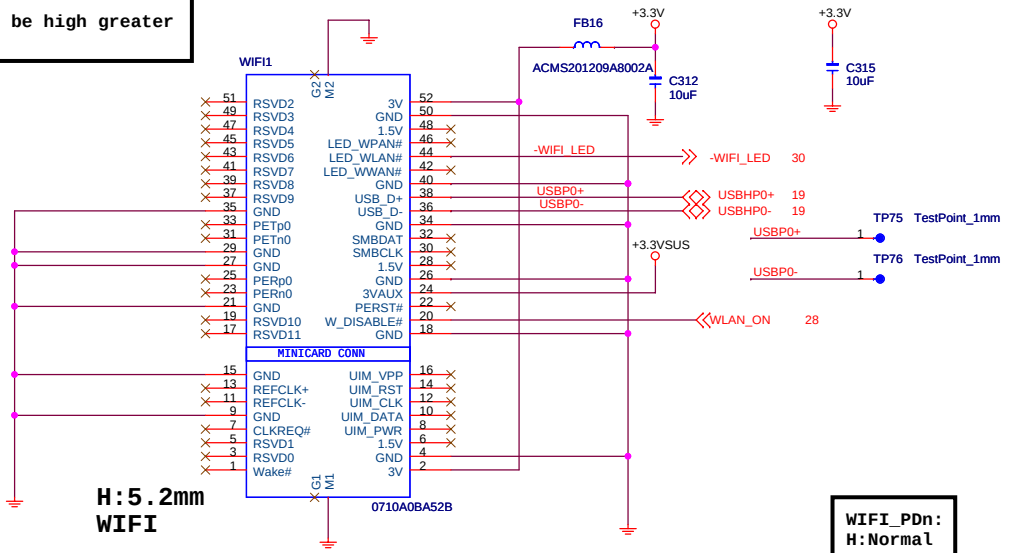
Note: Connector is inverse of the Touch PAD module.

WLAN LED



BT_RESET (Pin41):
Input pin, Reset if high, must be high greater than 5ms to reset.



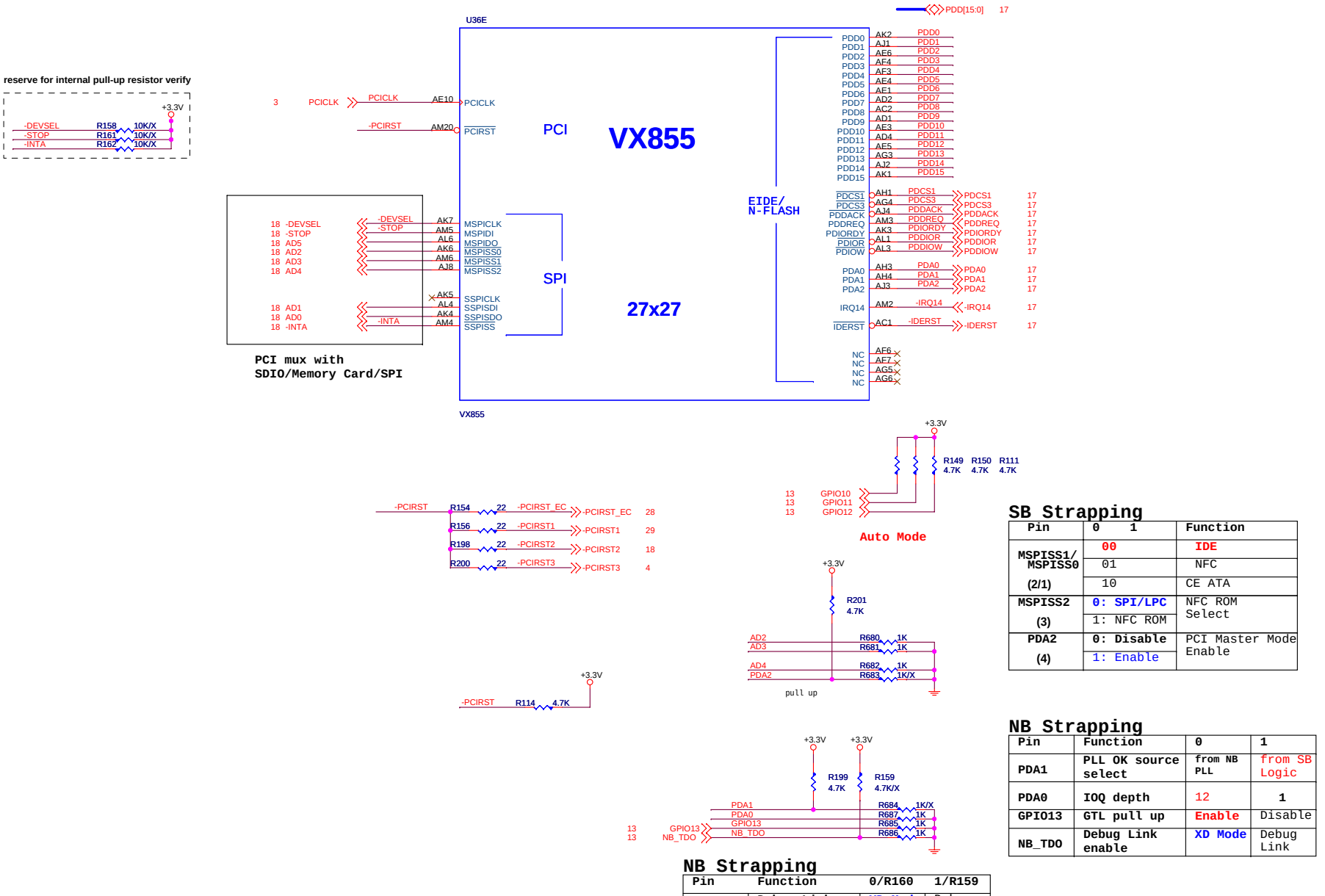


H:5.2mm
WIFI

WIFI_PDn:
H:Normal
L:Pown
Down

VIA TECHNOLOGIES INC.

Title	MICRO PAD,WiFi	
Size	Document Number VT6549B2	Rev 1.0
Date: Wednesday, July 15, 2009	Sheet 15 of 35	



SB Strapping

Pin	0 1	Function
MSPISS1/ MSPISS0 (2/1)	00	IDE
	01	NFC
	10	CE ATA
MSPISS2 (3)	0: SPI/LPC	NFC ROM Select
	1: NFC ROM	
PDA2 (4)	0: Disable	PCI Master Mode Enable
	1: Enable	

NB Strapping

Pin	Function	0	1
PDA1	PLL OK source select	from NB PLL	from SB Logic
PDA0	IOQ depth	12	1
GPIO13	GTL pull up	Enable	Disable
NB_TDO	Debug Link enable	XD Mode	Debug Link

NB Strapping

Pin	Function	0/R160	1/R159
NB_TDO	Debug Link enable	XD Mode	Debug Link

VIA TECHNOLOGIES INC.

Title: VX855 PCI&SPI&PATA BUS

Size: A3 | Document Number: VT6549B2 | Rev: 1.0

Date: Wednesday, July 15, 2009 | Sheet 16 of 35

PATA to SATA HDD Master

1.8" HDD CONNECTOR Master

88SA8052

Marvell Install R374, FB18; remove FB26
JMICRON remove R374, install FB18, FB26
Sunplus Install R374, FB26; remove FB18

Marvell & JMICRON Install R373
Sunplus remove R2, install R366

Marvell R294 is 6.04K Ohm 1%
JMICRON R294 is 12K Ohm 1%
Sunplus R294 is 1K Ohm 1%

Sunplus install R818; remove R350
Marvell & JMICRON install R350;
remove R818

Sunplus remove R346
Marvell & JMICRON install R346

Marvell install R167, remove R171
JMICRON & Sunplus remove R167, R171

Marvell install R170, remove R169
JMICRON remove R170, R169
Sunplus install R169, remove R170

Marvell, Sunplus install R168,
remove R172
JMICRON install R172, remove R168

Marvell & JMICRON remove R387
install R375, R385, R386

Sunplus install R387,
remove R375, R385, R386

Marvell & JMICRON install R195, R414;
remove R191, R415

Sunplus remove R195, R191, R414, R415

CLKSLE0 CLKSLE1
25MHZ 1 0

0= Disable SSC
1= enable SSC

0= Device0
1= Device1

reserve for SATA 3G 1.3V
VOUT=1.25*(1+R2/R1)+Iadj*R2

SPIF223A

80-pin hdd
cable type.
ask BIOS to Fix

reserve for internal pull-up resistor verify

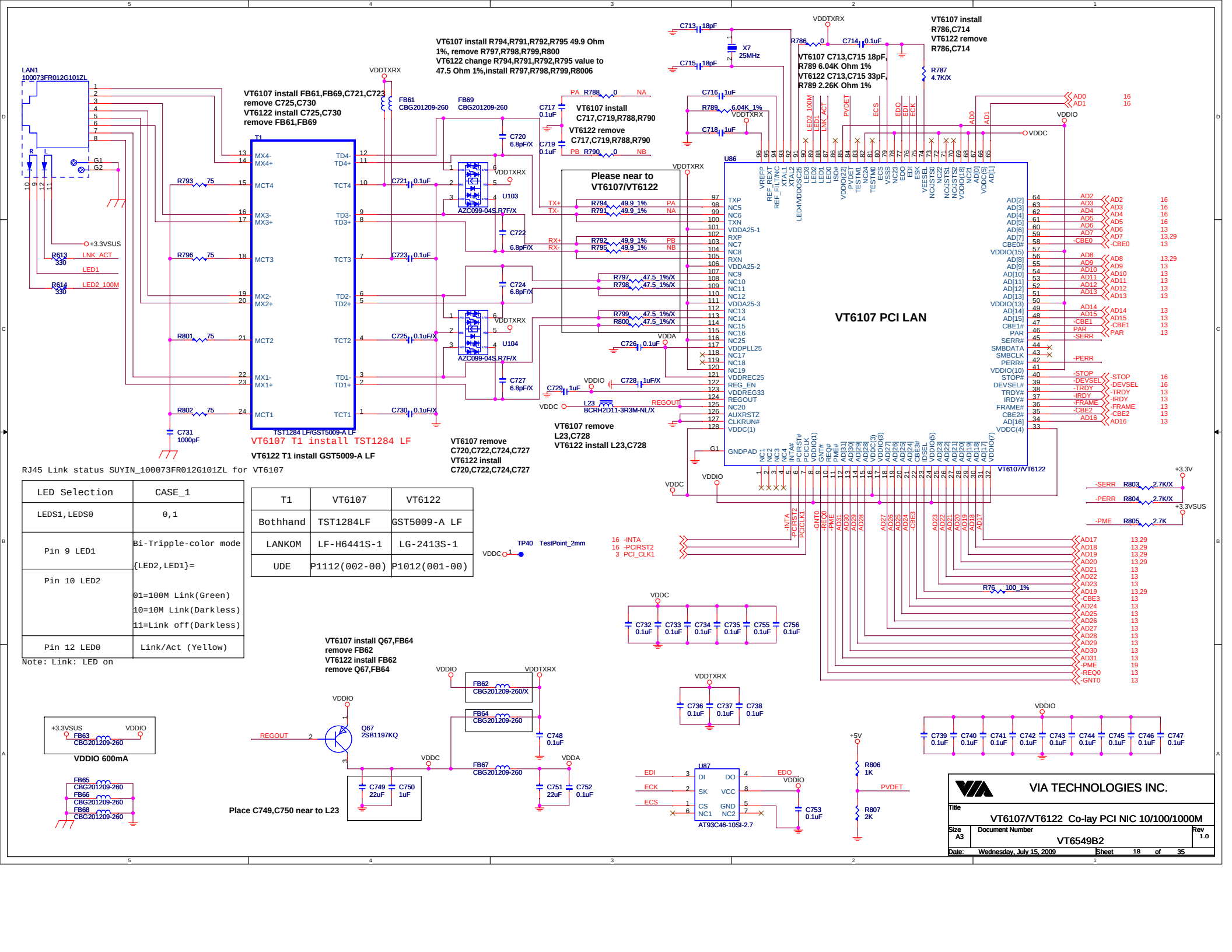
Marvell & JMICRON install R819,
remove R821, Q68, C760
Sunplus install R821, Q68, C760;
remove R819

VIA TECHNOLOGIES INC.

Title: PATA TO SATA 1

Size: C | Document Number: VT6549B2 | Rev: 1.0

Date: Wednesday, July 15, 2009 | Sheet 17 of 35



RJ45 Link status SUYIN_100073FR012G101ZL for VT6107

LED Selection	CASE_1
LEDS1,LEDS0	0,1
Pin 9 LED1	Bi-Tripple-color mode {LED2,LED1}=
Pin 10 LED2	01=100M Link(Green) 10=10M Link(Darkless) 11=Link off(Darkless)
Pin 12 LED0	Link/Act (Yellow)

Note: Link: LED on

T1	VT6107	VT6122
Bothhand	TST1284LF	GST5009-A LF
LANKOM	LF-H6441S-1	LG-2413S-1
UDE	P1112(002-00)	P1012(001-00)

Size	Document Number	Rev
A3	VT6549B2	1.0

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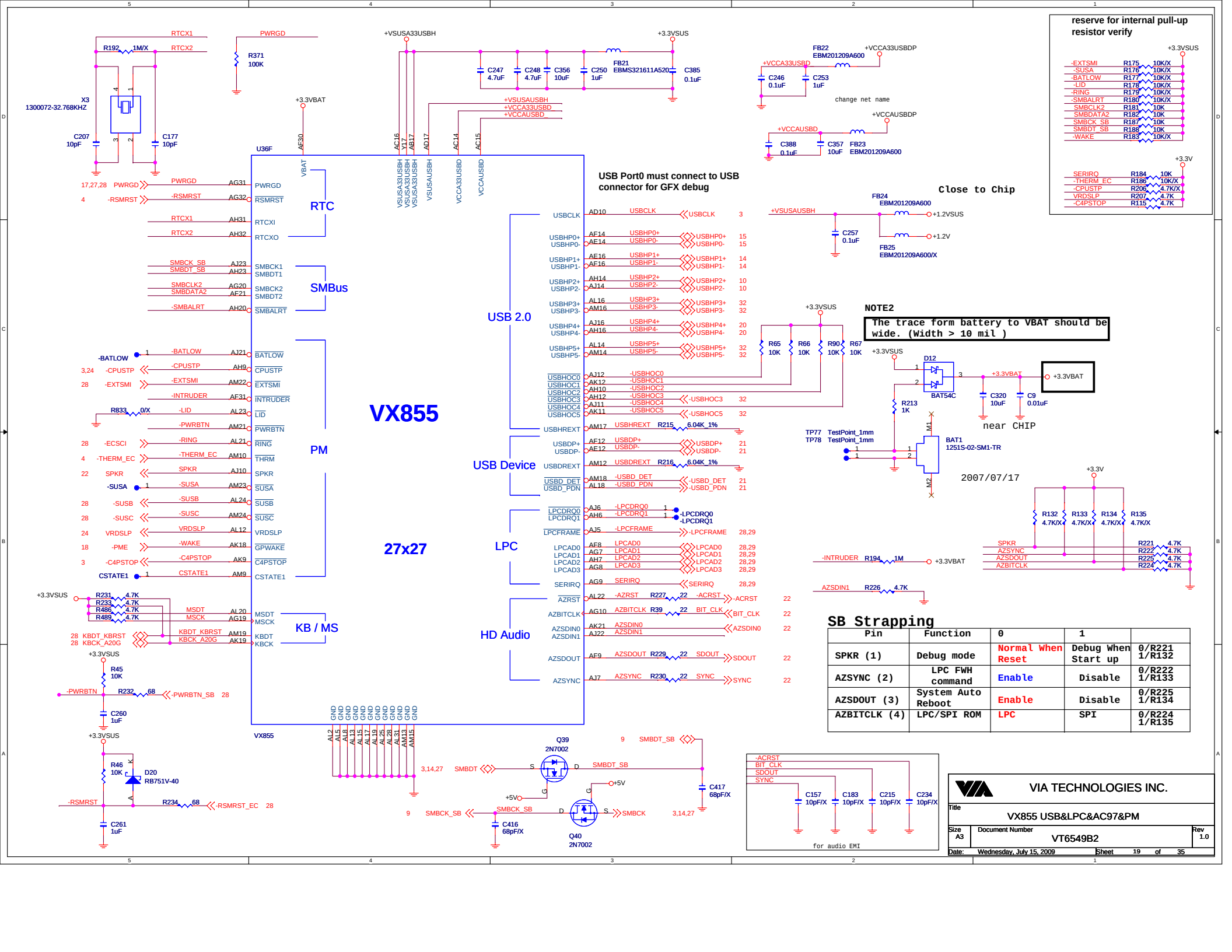
VX855
27x27
U36F
RTC
SMBus
PM
USB 2.0
USB Device
LPC
HD Audio
KB / MS
USB Port0 must connect to USB connector for GFX debug
Close to Chip
reserve for internal pull-up resistor verify
NOTE2
The trace form battery to VBAT should be wide. (Width > 10 mil)
near CHIP
2007/07/17
change net name
for audio EMI
SB Strapping
Pin | Function | 0 | 1 | 0/R221 1/R132
SPKR (1) | Debug mode | Normal When Reset | Debug When Start up
AZSYNC (2) | LPC FWH command | Enable | Disable | 0/R222 1/R133
AZSDOUT (3) | System Auto Reboot | Enable | Disable | 0/R225 1/R134
AZBITCLK (4) | LPC/SPI ROM | LPC | SPI | 0/R224 1/R135
VIA TECHNOLOGIES INC.
Title
VX855 USB&LPC&AC97&PM
Size A3
Document Number VT6549B2
Rev 1.0
Date: Wednesday, July 15, 2009
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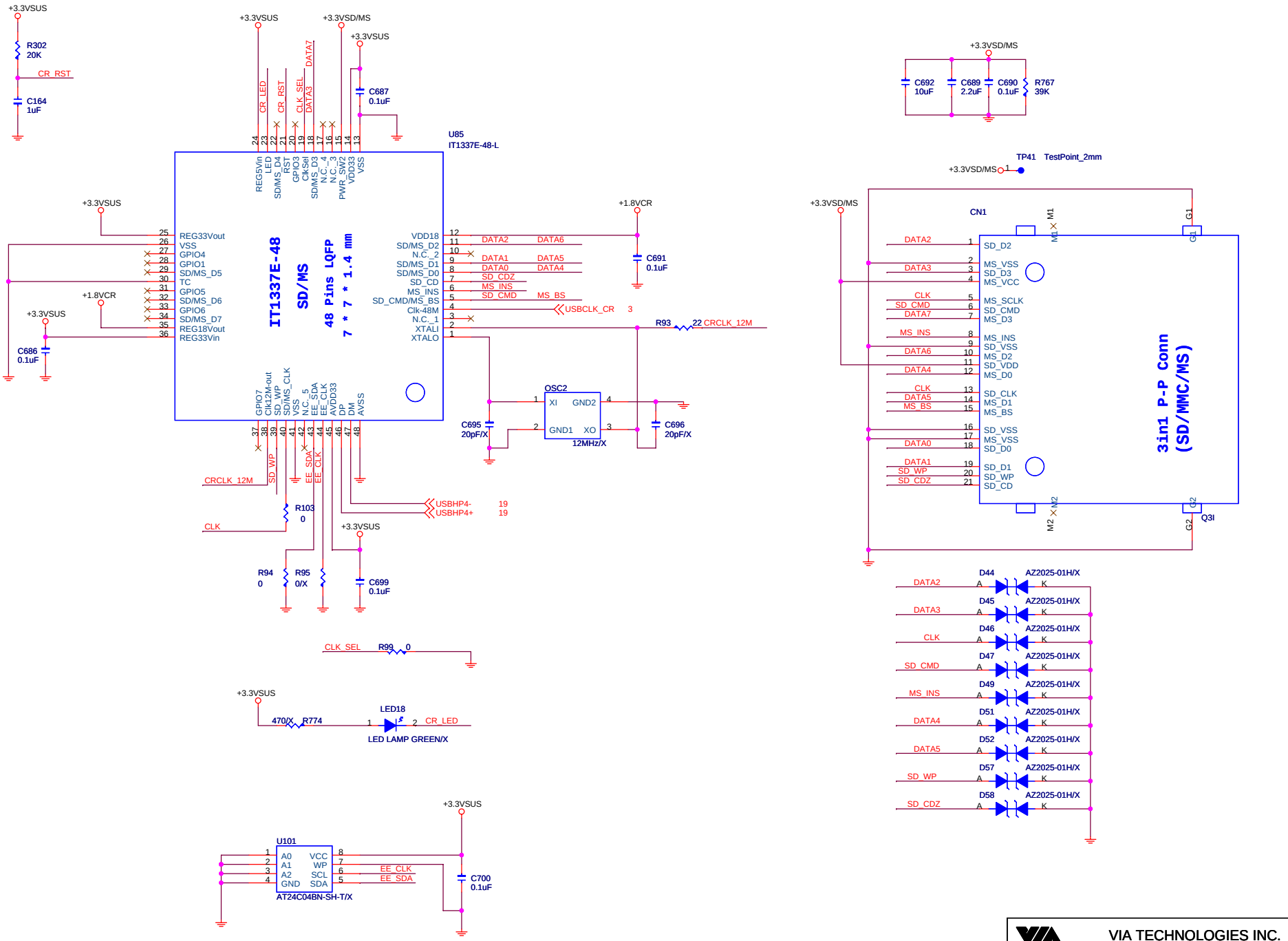
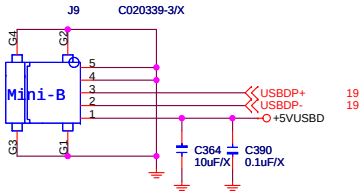
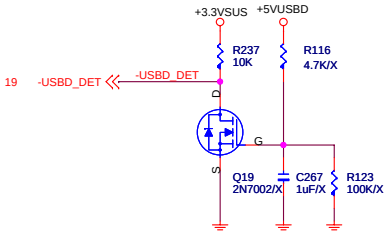
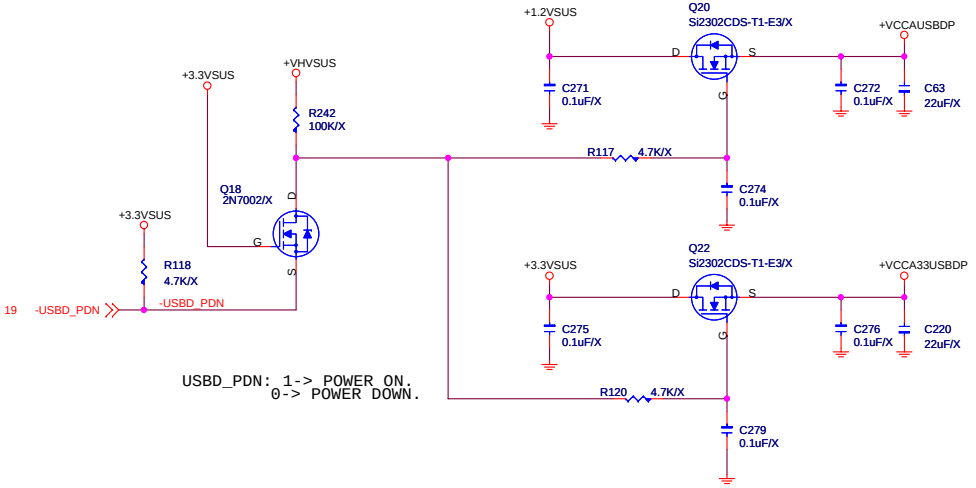


VIA TECHNOLOGIES INC.	
Title	IT1337 USB Card Reader
Size: Custom	Document Number: VT6549B2
Rev	1.0
Date: Wednesday, July 15, 2009	Sheet 20 of 35

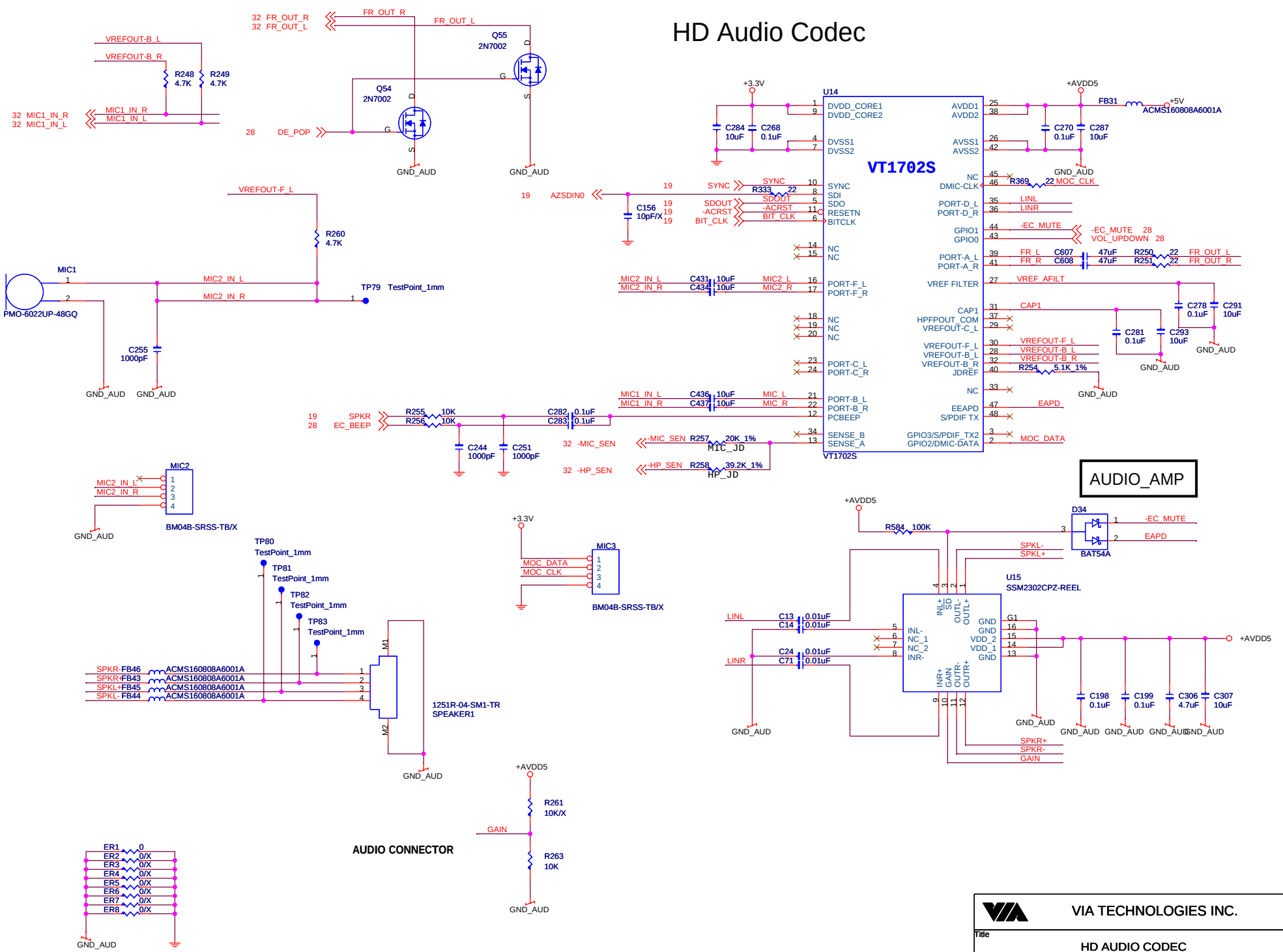




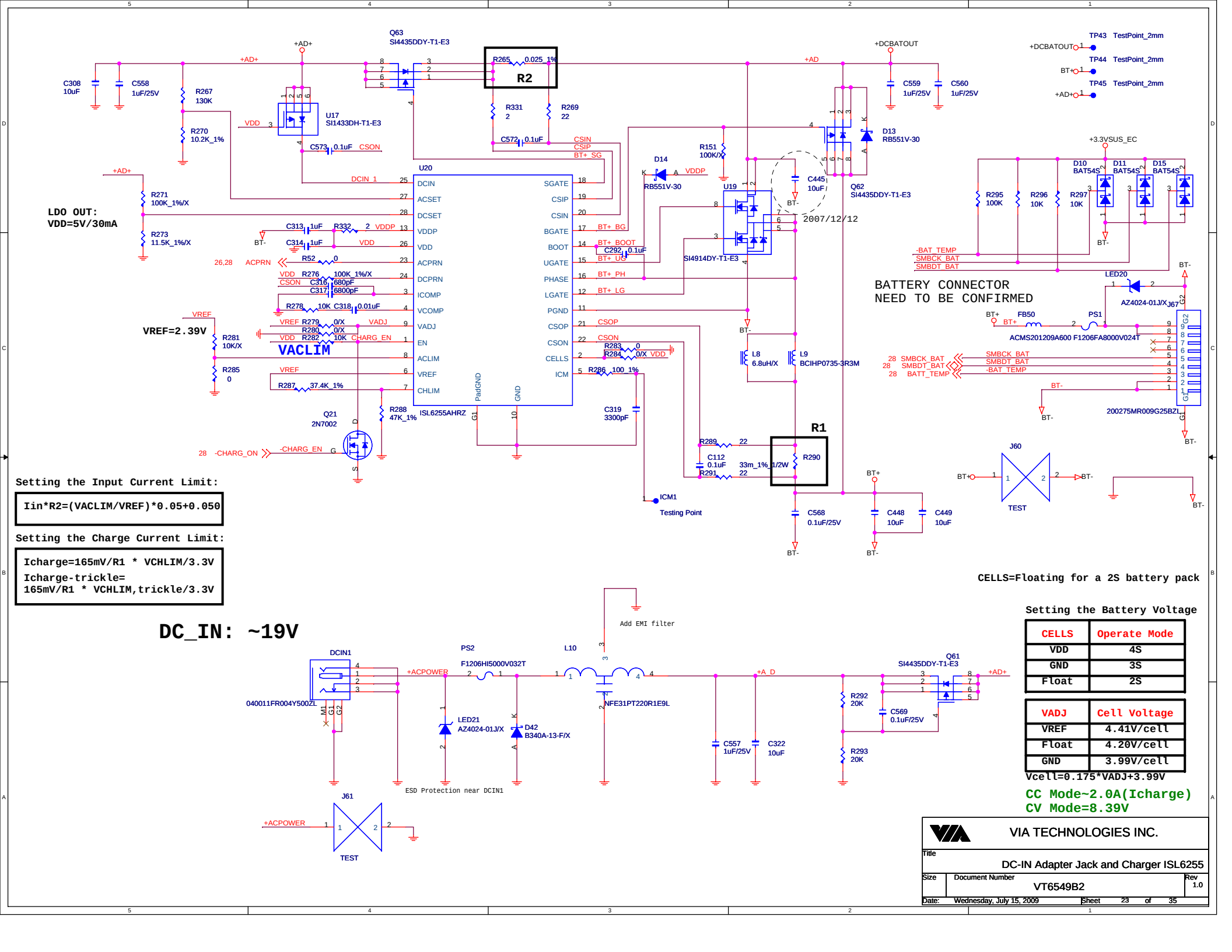


VIA TECHNOLOGIES INC.		
Title: USBH/D2.0		
Size: A3	Document Number: VT6549B2	Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 21 of 35	

HD Audio Codec



VIA TECHNOLOGIES INC.			
Title: HD AUDIO CODEC			
Size	Document Number: VT6549B2		Rev: 1.0
Date: Wednesday, July 15, 2009	Sheet 22 of 35		


LDO OUT:
VDD=5V/30mA
VREF=2.39V
VACLIM
BATTERY CONNECTOR
NEED TO BE CONFIRMED
2007/12/12
Setting the Input Current Limit:
Iin*R2=(VACLIM/VREF)*0.05+0.050
Setting the Charge Current Limit:
Icharge=165mV/R1 * VCHLIM/3.3V
Icharge-trickle=
165mV/R1 * VCHLIM,trickle/3.3V
DC_IN: ~19V
CELLS=Floating for a 2S battery pack
Setting the Battery Voltage
CELLS | Operate Mode
VDD | 4S
GND | 3S
Float | 2S
VADJ | Cell Voltage
VREF | 4.41V/cell
Float | 4.20V/cell
GND | 3.99V/cell
Vcell=0.175*VADJ+3.99V
CC Mode~2.0A(Icharge)
CV Mode=8.39V
VIA TECHNOLOGIES INC.
Title
DC-IN Adapter Jack and Charger ISL6255
Size
Document Number
VT6549B2
Rev
1.0
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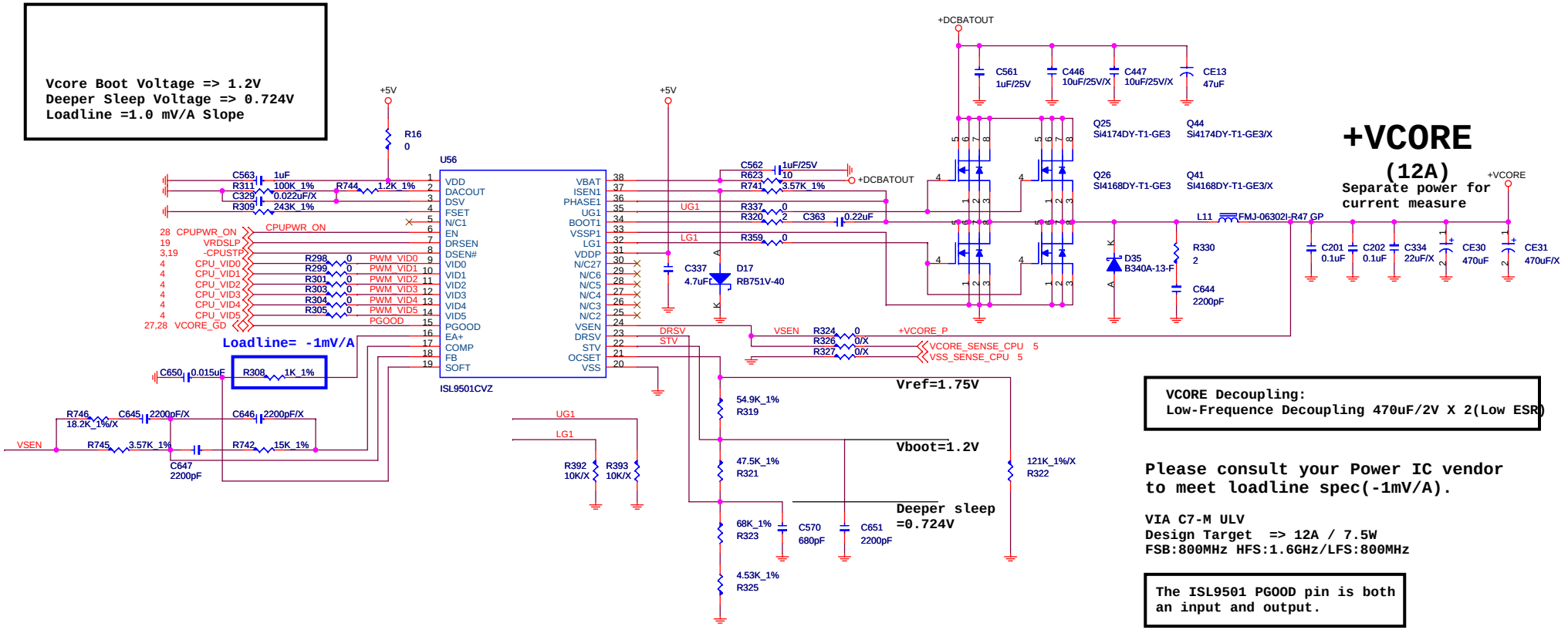
CPU VCORE POWER: +VCORE

Vcore Boot Voltage => 1.2V
Deeper Sleep Voltage => 0.724V
Loadline =1.0 mV/A Slope



+VCORE (12A)

Separate power for current measure

VCORE Decoupling:
Low-Frequence Decoupling 470uF/2V X 2(Low ESR)

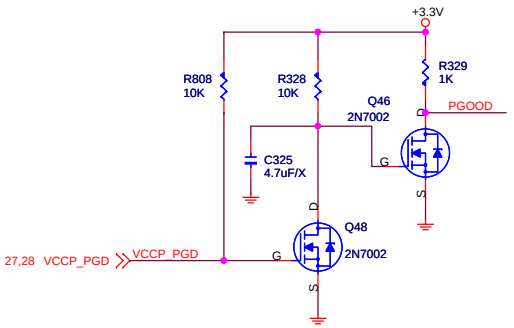
Please consult your Power IC vendor to meet loadline spec(-1mV/A).

VIA C7-M ULV
Design Target => 12A / 7.5W
FSB:800MHz HFS:1.6GHz/LFS:800MHz

The ISL9501 PGOOD pin is both an input and output.

VIA C7-M ULV Processor(March/2007)

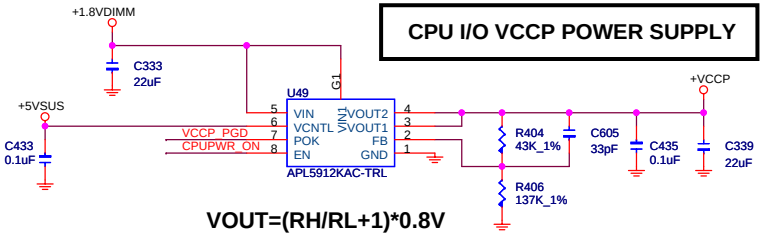
CPU TYPE	FSB (MHz)	P-STATE		Deeper Sleep C4	HFM / HFM_V POWER
		HFM / HFM_V	LFM / LFM_V		
VIA C7-M ULV 1.6GHz	800	1.6GHz / 988mV	800MHz / 796mV	0.724V	8.0 W
* VIA Nano ULV 1G+Hz	800				



SET 1.05V

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
* 1	1	0	1	1	0	0.844
1	1	1	0	0	1	0.796
1	1	1	1	0	0	0.748

CPU I/O VCCP POWER SUPPLY



VOUT=(RH/RL+1)*0.8V

VIA TECHNOLOGIES INC.

Title: CPU Vcore ISL9501

Size	Document Number	Rev
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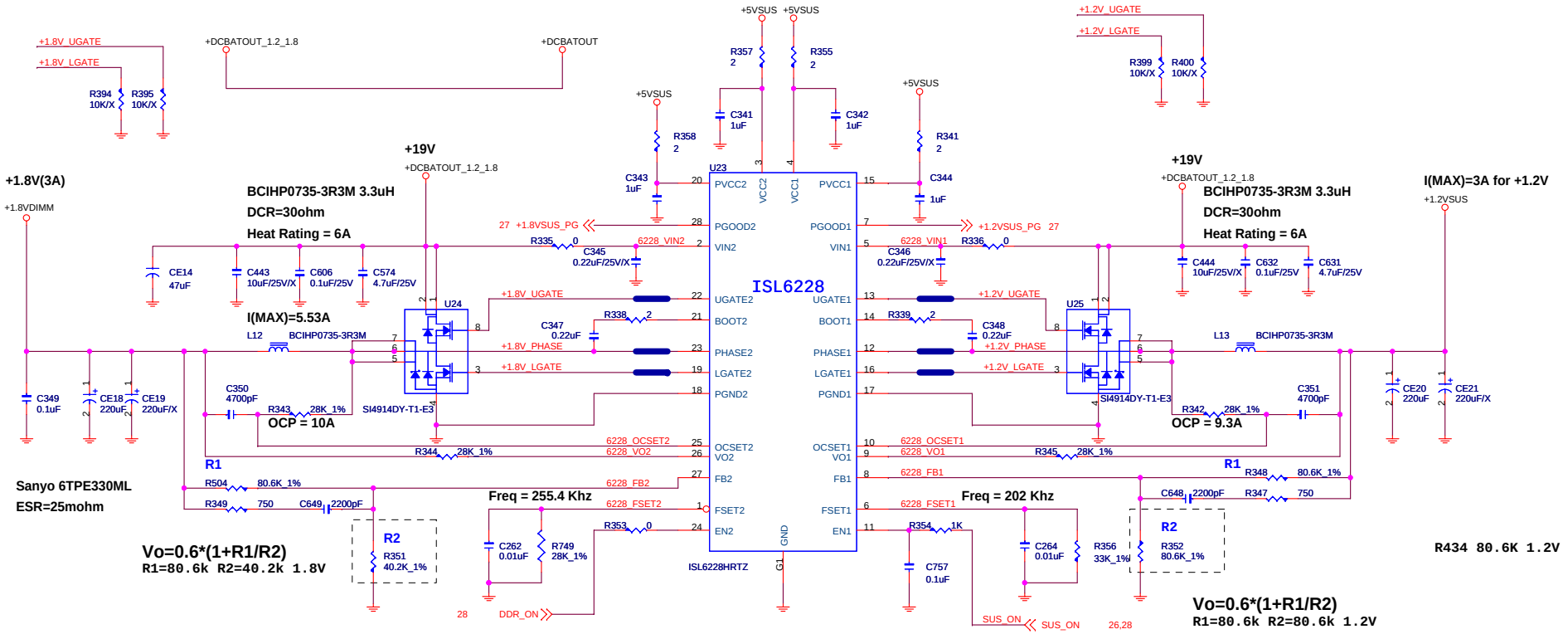

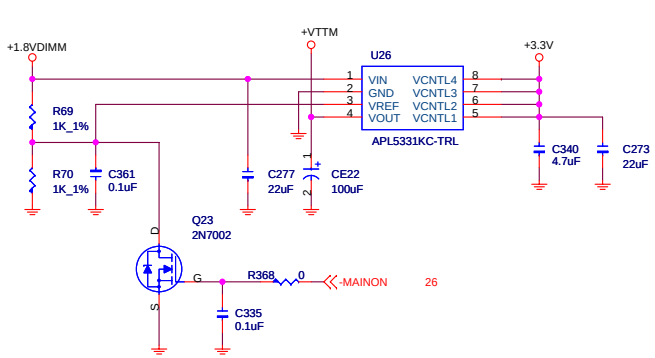

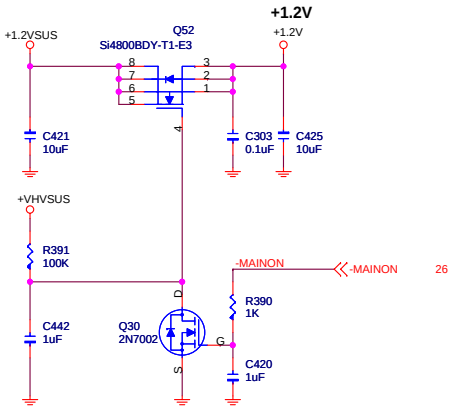

VIA TECHNOLOGIES INC.		
Title: +1.8V/+1.2/0.9V		
Size: A3	Document Number: VT6549B2	Rev: 1.0
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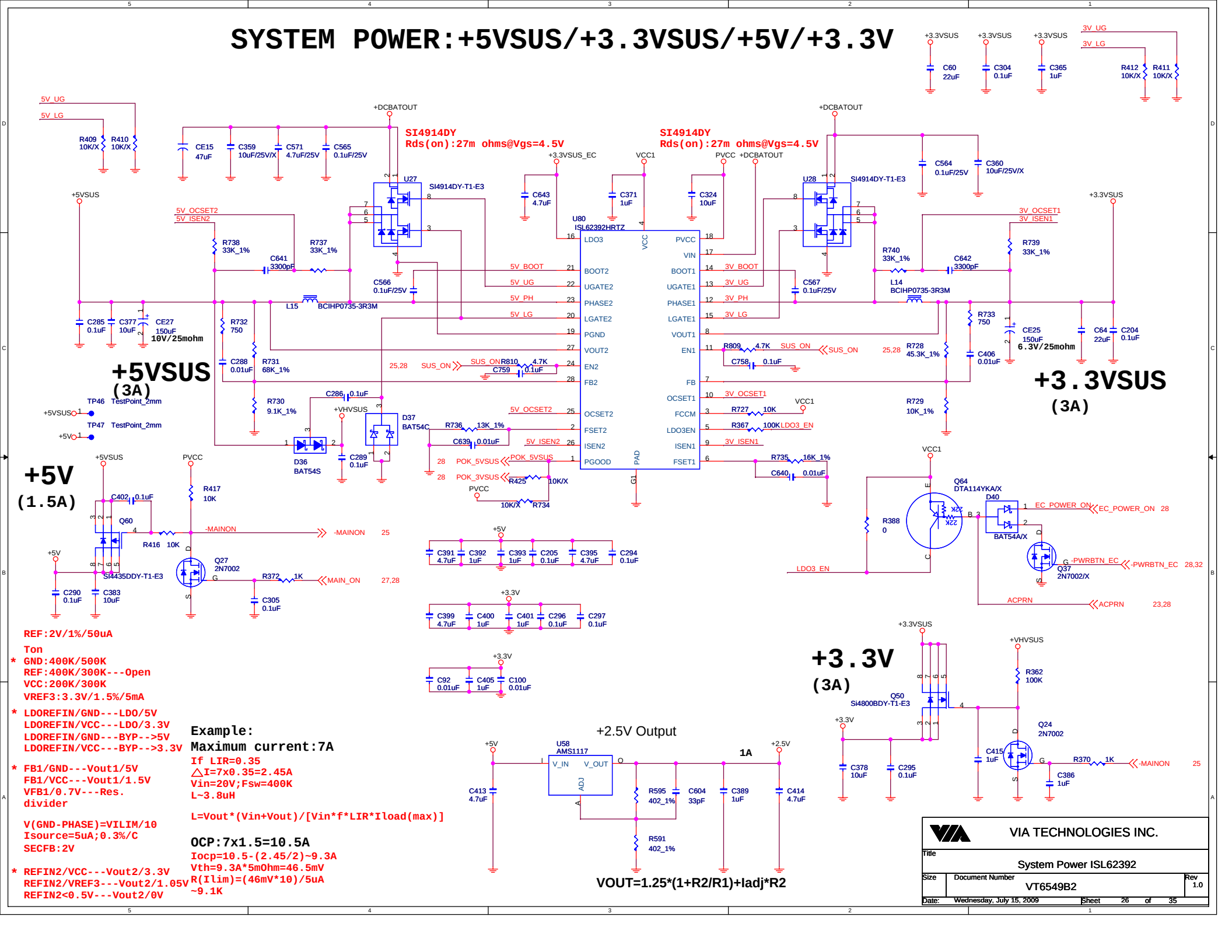
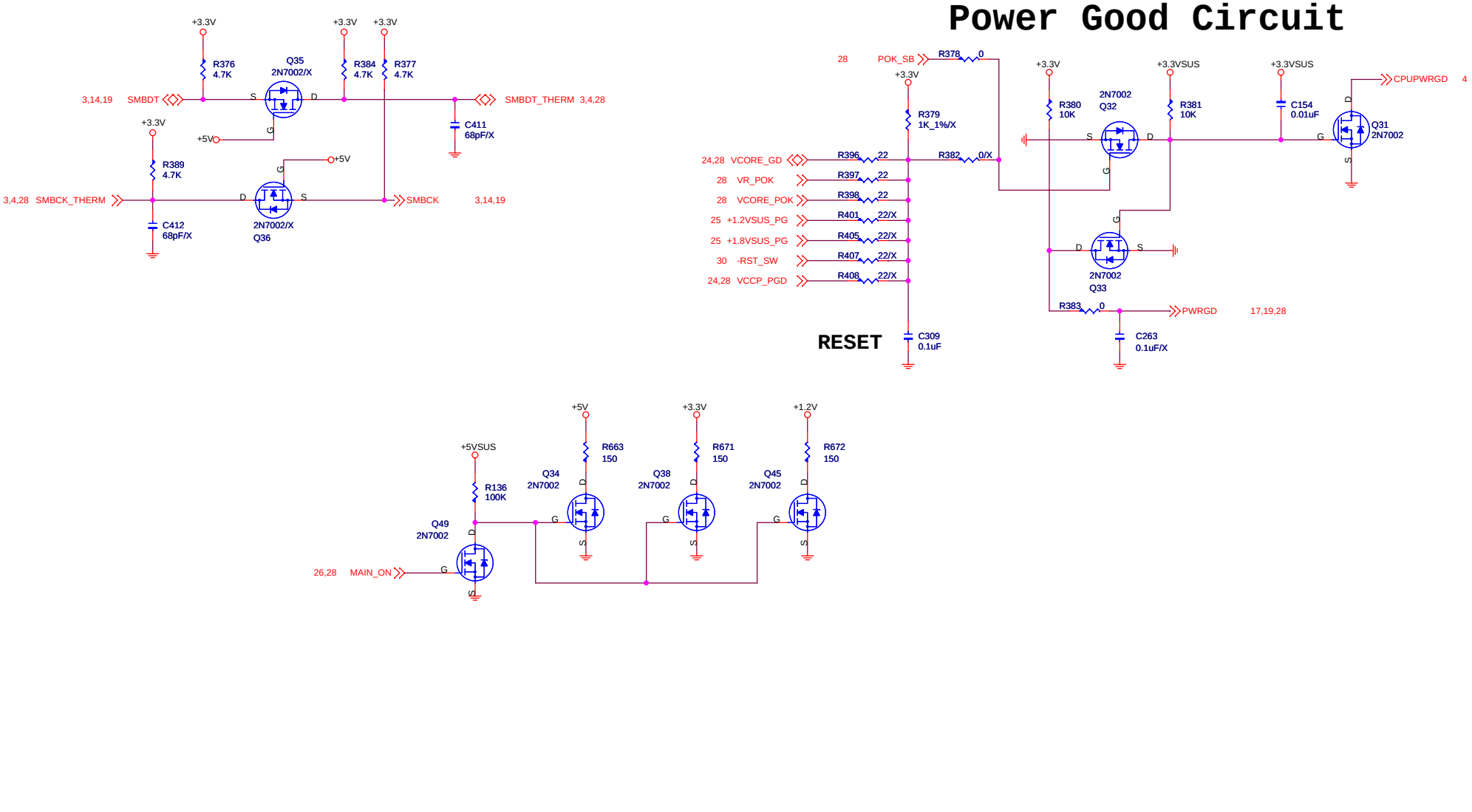
SYSTEM POWER:+5VSUS/+3.3VSUS/+5V/+3.3V



Power Good Circuit



VIA TECHNOLOGIES INC.		
Title: PWRGD Circuit		
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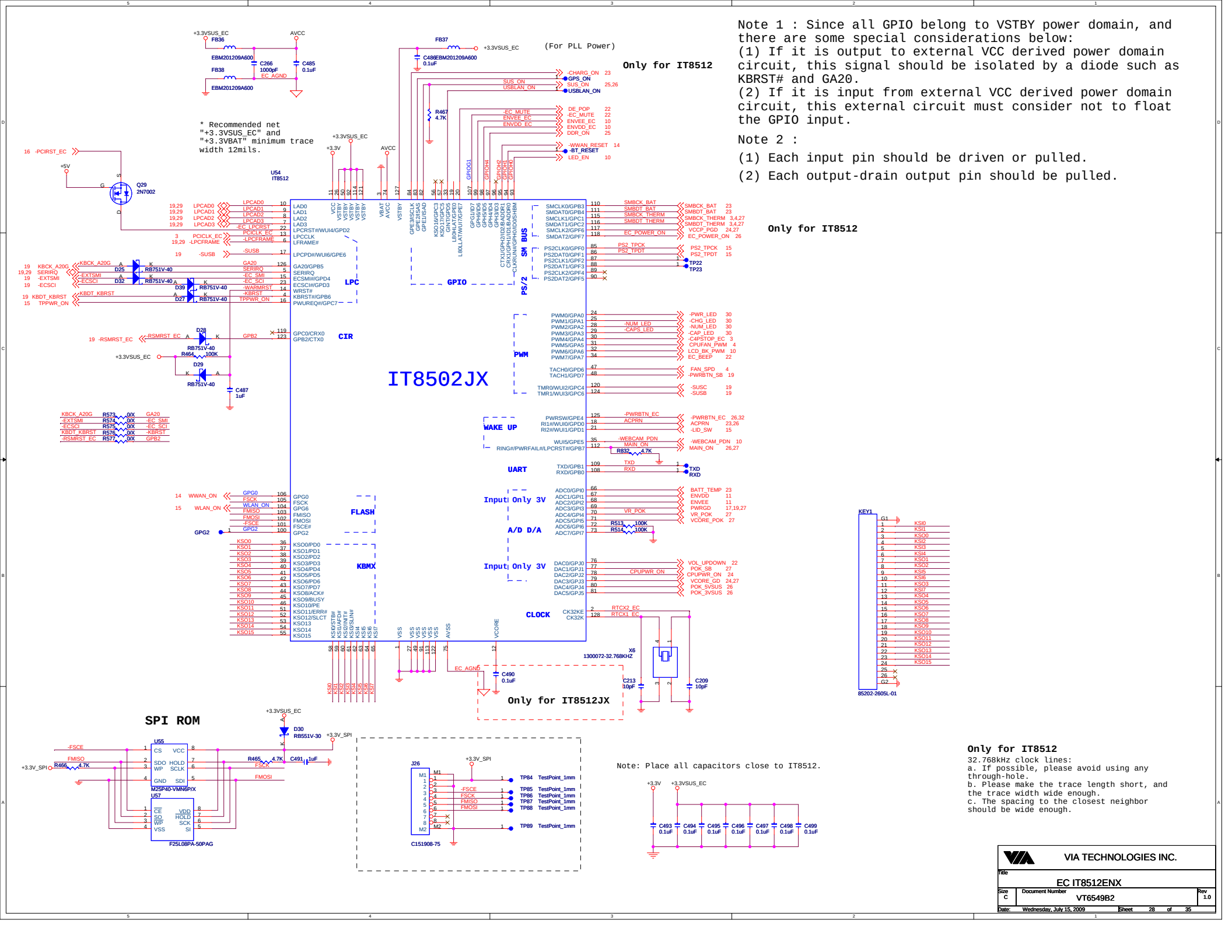
IT8502JX
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
* Recommended net "+3.3VSUS_EC" and "+3.3VBAT" minimum trace width 12mils.
(For PLL Power)
Only for IT8512
Only for IT8512JX
SPI ROM
Note: Place all capacitors close to IT8512.
Only for IT8512
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
VIA TECHNOLOGIES INC.
EC IT8512ENX
VT6549B2
Wednesday, July 15, 2009

Flash EPROM download from KBMX interface enable method(EPP mode).
(Select one of below.)
1. Enable by LPT Cable for IT8512(See Spec. for Detail.)

This page's circuit can be a independent daughter board.

Subject to Change Without Notice.

VIA TECHNOLOGIES INC.		
Title: Board to Board		
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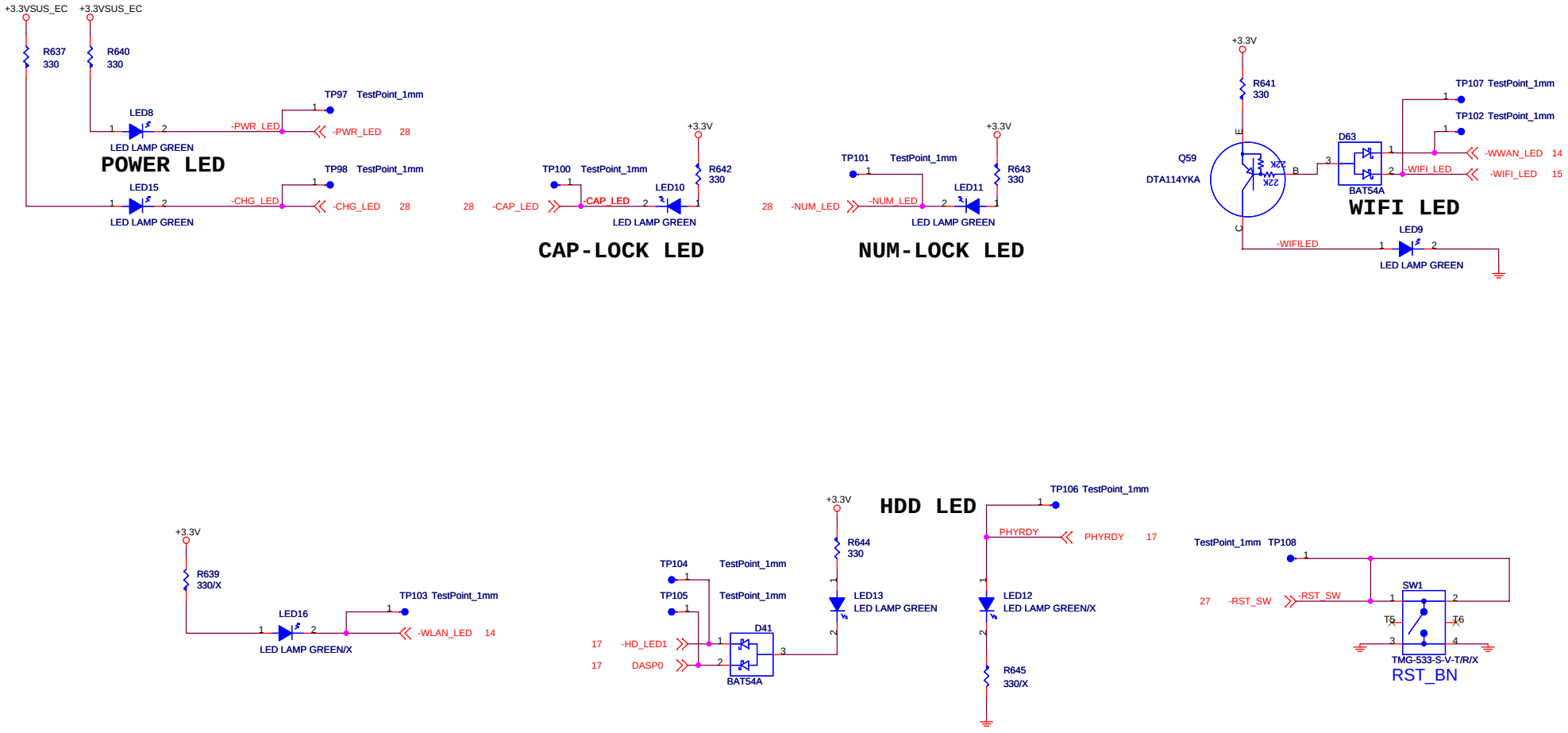

VIA TECHNOLOGIES INC.	
Title	LED & Buttom
Size: Custom	Document Number: VT6549B2
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VIA TECHNOLOGIES INC.

Title

Debug only

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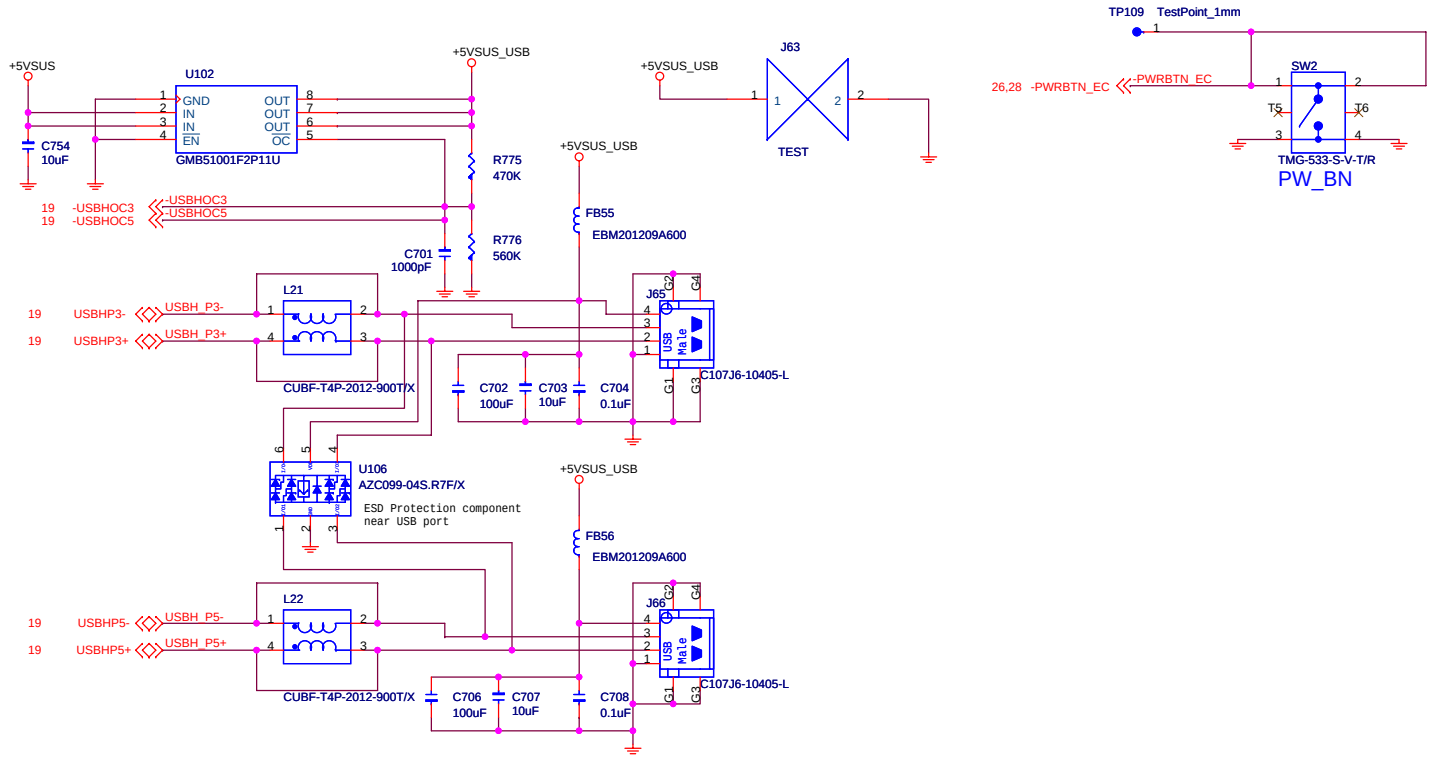

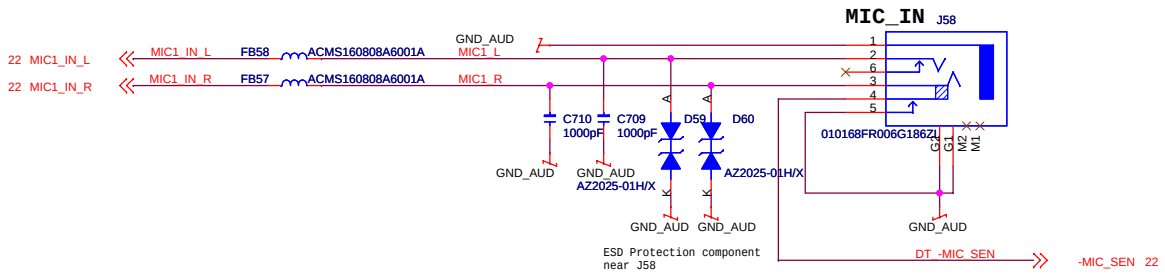

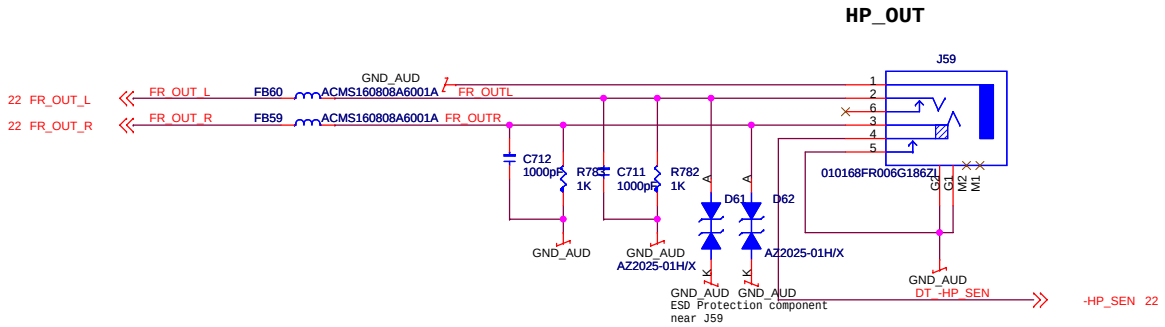

VIA TECHNOLOGIES INC.		
Title: USER		
Size: Custom	Document Number: VT6549B2	Rev: 1.0
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VIA TECHNOLOGIES INC.

Title

Debug only

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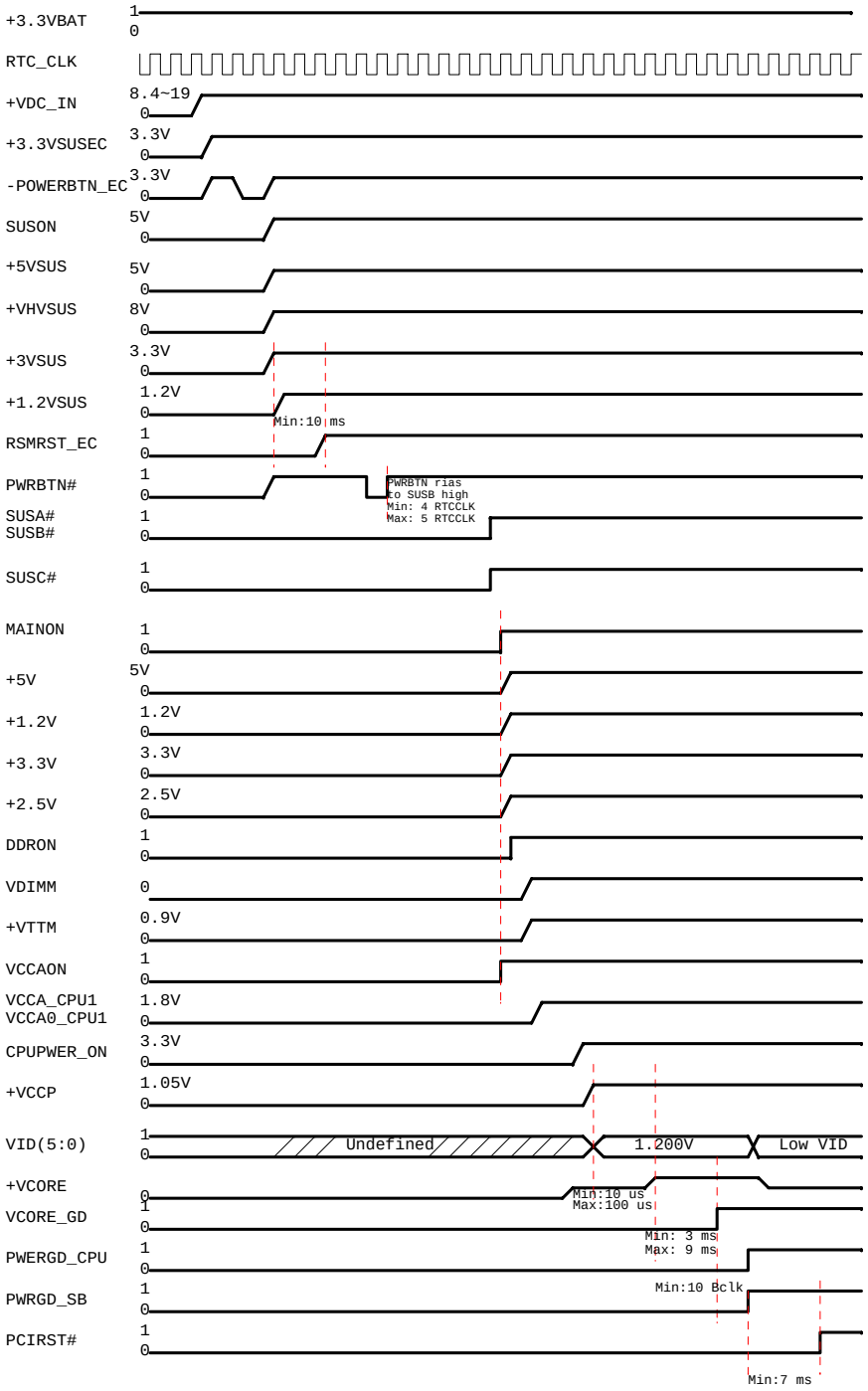
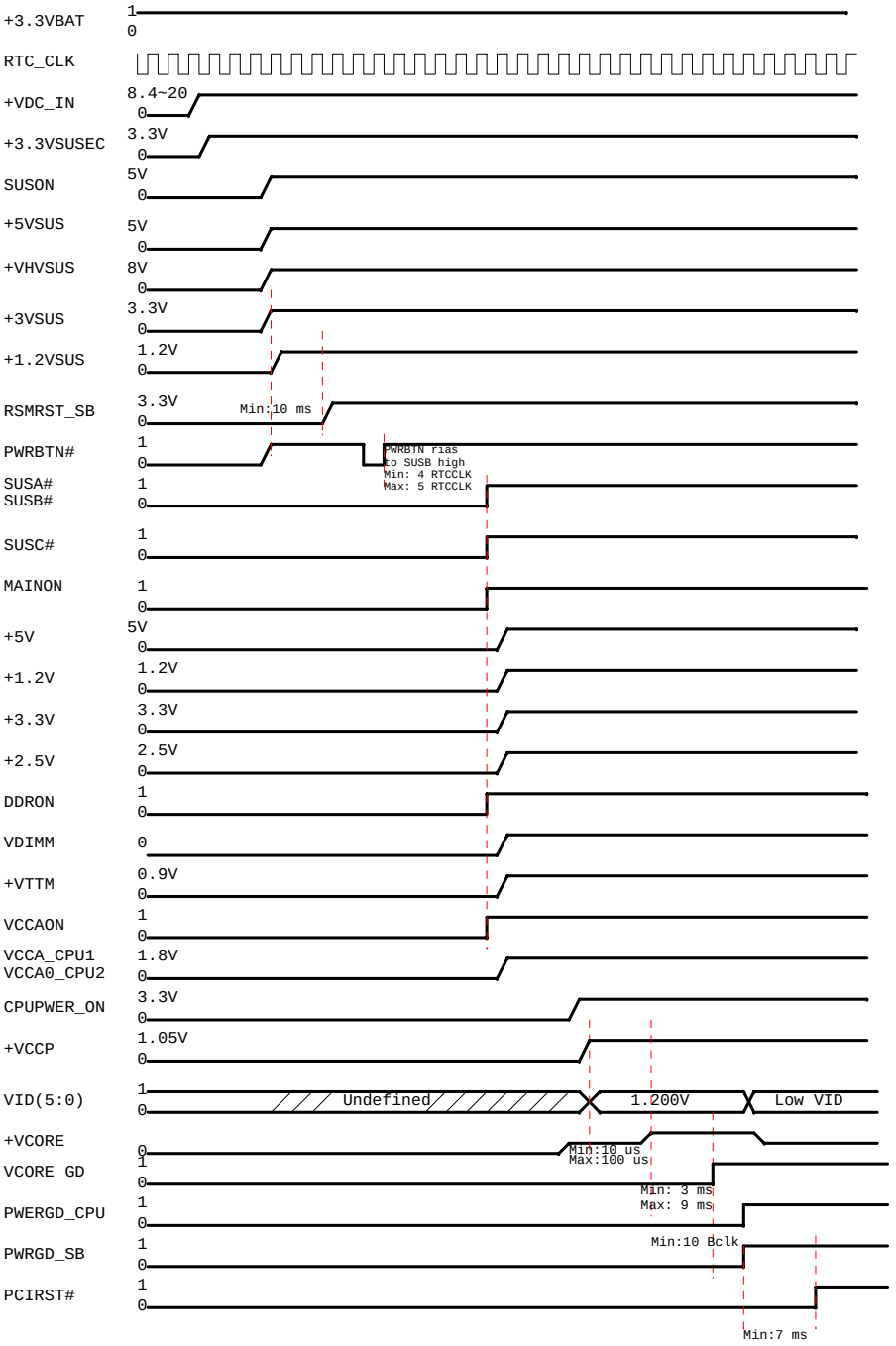
Power onsequence with EC



Power onsequence without EC



VIA TECHNOLOGIES INC.

Title: Power on sequence

Size	Document Number	Rev
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VT6549A rework
1. U55換8M SPI ROM
2. R367.2 改接到 R727.2
3. U58.I 及 C413.2改接到 C205.1
4. 換SATA connector
5. FAN1.2及FAN1.3加diode
6. SUS_ON加4.7K 0603到地
7. Remove R185
8. 上R189
9. RemoveR598
10. R334.2改到R383.2
11. Remove R281
12. R285改 0 ohm
13. R265改25m ohm
14. Add a diode on R46
15. R684改pull up 3.3V
16. Remove J41
17. Short U63 pin5 and pin6
18. R417 改接 PVCC
19. Remove R261 and put it on R263

VT6549A to VT6549B
1. PCI NIC
2. USB Card Reader

VIA TECHNOLOGIES INC.

Title: History

Size	Document Number	Rev
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