Arasan
The Bus Stops Here

PRODUCT OVERVIEW

SD 2.1 / eMMC 4.4 / CE-ATA Memory Controller IP

Features

SD 2.1
- Meets SD 2.1 Physical Layer Specification
- Supports SPI, 1-bit, 4-bit SD modes
- Supports SD and SDHC cards
- Host clock rate 0-50MHz
- Addresses cards up to 32GB
- Comfortable erase mechanism

MMC 4.4 (eMMC)
- Complies to Multimedia Card System Specification Version 4.4 (eMMC)
- Supports 1-, 4-, or 8-bit MMC data bus
- Supports frequencies up to 52Mhz, DDR mode peak bandwidth is 104MBps
- Controller supports hardware reset pin(RST_n)
- Supports Partition Management features with enhanced storage option
- Supports memory size over 2GB
- Supports both Power-on boot mode and alternate boot mode
- Sector address allows host to access high capacity card
- Performs Secure Erase, Secure TRIM and TRIM operations
- Introduce of New Secure Features, Replay Protected Memory Block(RPMB) access control

CE_ATA
- Complies to CE_ATA Digital Protocol Specification Version 1.1
- Supports block lengths or sector sizes of 512, 1024, and 4096 bytes
- Command complete signaling

Common SD / eMMC Features
- Card write protection (power on,temporary and permanent) and password features
- Supports block lengths or sector sizes of 512, 1024, and 2048 bytes
- Hot insertion of cards
- Memory error correction mechanisms

AHB
- Complies to AMBA specification version 2.0.
- Supports incremental burst transfers in DMA mode
- Supports register transfer in non-DMA mode
- Supports retry and split

Overview

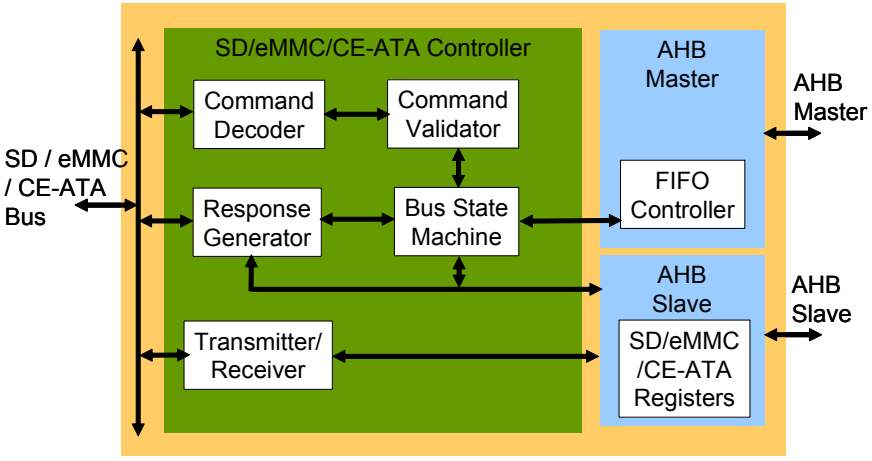
The rapid growth in features and functionality of compact and portable electronics requires a corresponding increase in memory to store program code and user data. To address this need Arasan has developed a flexible multi-protocol memory controller IP that combines Secure Digital (SD), MultiMedia Card (MMC) and CE-ATA Memory Controllers.

Arasan's SD / eMMC / CE-ATA Memory Controller IP is compliant with the SD 2.1 Physical Layer, MMC 4.4 (eMMC) and CE-ATA 1.1 standards. The controller provides a bandwidth of up to 25 MBps in SD mode and 104MBps in MMC mode. A NAND flash or other storage media can be connected to the AHB bus on this Memory Controller. A Host system can use a standard SD / eMMC / CE-ATA bus to access memory irrespective of the underlying memory technology. The controller supports all of the SD features such as content protection, write protection, correction of memory errors and password based card lock, un-lock.

CE-ATA is based on the MMC electrical interface and uses five MMC commands to access storage media (HDD). The Controller handles CE-ATA commands such as CMD39, CMD60, and CMD61. The Memory Controller operates at a maximum frequency of 52 MHz. The interface supports SD 1-bit, 4-bit modes and MMC 1-bit, 4-bit, and 8-bit modes. It supports the newer eMMC functions such as multiple boot mechanisms, card memory partitions, replay protected memory block and secure erase. eMMC supports power-on booting without the upper level of software driver. An explicit sleep mode allows the host to instruct the controller to directly enter the low power sleep mode.

Arasan provides a "Total IP Solution" for the SD / eMMC / CE-ATA Memory Controller consisting of RTL source files, synthesis scripts, test environment and documentation backed by Arasan's World-class customer support.

SD / eMMC / CE-ATA Memory Controller IP Core Functional Block



Version 1.0

SD 2.1 / eMMC 4.4 / CE-ATA Memory Controller IP

SD / eMMC / CE-ATA Controller:

The controller comprises of the Command Decoder, Command Validator, Response Generator, Receiver, Transmitter, and Bus State Machine. The Command Decoder registers the 48-bit command for all modes including MMC 1-bit, 4-bit, and 8-bit modes. It also verifies the CRC for received commands. The Response Generator sends appropriate responses for received commands in all modes of operation. The Transmitter and Receiver block handles the data transactions. Abort protocol is supported. The Command Validator validates the received commands based on the state of the controller. This block checks for parameter errors, address errors and errors in the argument field of the command. It also handles password authentications and is responsible to check if the card is locked or unlocked. The Bus State Machine handles bus states described in the SD, eMMC, CE-ATA specification. The eMMC compliant controller supports additional features such as power-on boot mode, sleep mode, and sector address mapping for high-capacity card access.

AHB/APB Interface:

The AHB interface consists of the master interface and slave interface. The AHB slave is used by external processor to configure the SD / eMMC /CE-ATA Memory controller, and for programing the control of data transfer between the it and application's memory. The AHB master interface is used to transfer packets between the internal FIFOs and application memory. Before an AMBA AHB transfer can commence, the bus master must grant access to the bus. This process is started by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted the use of the bus. A granted bus master starts an AHB transfer by driving the address and control signals.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Reuse Methodology Manual guidelines (RMM) compliant verilog code

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

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Data Sheet Links:

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